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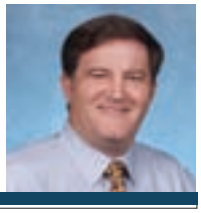
Interoperability: The dilemma

Is the DoD doing enough to enable standards in embedded computing?



By Jerry Gipper

The interoperability of COTS electronic modules is a common problem that faces anyone developing a complex embedded computing platform. Getting all of the modules to work together is a formidable integration challenge for system integrators. Components and modules need to connect easily and quickly into the system: plug-and-play, not *plug-and-fight.* Unfortunately, though industry standards may exist for these modules, the interoperability of the devices is not always as it should be. Are design standards enough? Should something else be done to ensure compatibility and interoperability? Should the standards be strengthened or new standards added?

Integrators are under program deadlines and are pressed to complete the system integration as quickly as possible. The bottom line is that defense program integrators want common, interoperable, yet flexible standards for their electronic programs. Most of these modules are already designed to their relative industry standard yet they still fail to interoperate in many cases, often because the standards leave a lot to interpretation or are incomplete in key areas.

Pressure on system integrators is only increasing because the current users of defense embedded computing systems are young and very computer savvy. They know how to use computers and expect the latest in computing technology. Their experience with Windows-based PCs has become relatively pleasant over the years as PCs have become much better at plug-and-play. The large volume of users and devices has forced the PC industry to make improvements in integration. Standards such as USB and the Windows API have made adding devices to a PC very painless. New recruits are going to drive demand for the latest in technology advancements, as they will expect components and modules that quickly integrate with no or minimum difficulty.

Defense applications are often based on a combination of hardware and software that is uniquely developed or integrated for that specific application. They may be running one of dozens of real-time operating systems. They are using one or several different computer platforms. The applications are often custom developed from the ground up. The device interconnects often include some arcane military computer standard unique to defense applications and supported by, at best, only a handful of suppliers.

The Future Combat System (FCS) program (www.army.mil/fcs) is one example of what the U.S. Department of Defense (DoD) is doing to improve the interoperability situation. FCS is one of the most complex systems integration and development programs ever executed by the DoD. The FCS network allows the FCS Family-of-Systems (FoS) to operate as a cohesive system-of-systems where the whole of its capabilities is greater than the sum of its parts. The program's goal is to develop an evolving system *toolset* based on open system architectures and standards-based interfaces.

The scope of the FCS program includes the development of manned and unmanned systems and their integrating network, the integration of complementary and associated programs, and development of the underlying doctrine, organization, training, facilitization, and other functions needed to develop and field a fully functioning unit of action. This required a new approach to complex systems integration. The DoD's approach is to use a single, accountable lead systems integrator to integrate the FCS family of systems. This integrator has to optimize operational capability, maximize competition for systems development, ensure interoperability, and maintain commonality to reduce life-cycle cost.

Using a lead systems integrator does not solve the underlying problem though. You will still have multiple vendors competing with multiple variations of standards-based technology that will continue to make a nightmare of integrating all of the embedded computing technology. Open-system architectures and standards-based interfaces that are not interoperable will continue to drag down the integration. For example, the numerous choices in VMEbus technology are making it very challenging to select products from multiple vendors and ensure interoperability. Different processor, interconnect, and software API choices add even more to the challenge.

The DoD has also published a DoD Architecture Framework (DoDAF) document. This is a framework for development of a systems architecture or Enterprise Architecture (EA). All major DoD weapons and information technology system procurements are required to develop an EA and document that architecture using

the set of views prescribed in the DoDAF. The DoDAF also has broad applicability across the private, public, and voluntary sectors around the world. But is this enough? Figure 1 depicts the DoDAF architecture development process.

The DoD has a great start with the DoDAF but an opportunity exists to step up and work with the embedded community to drive what it expects. It must push unification and interoperability of standards for all to follow. It should team up with integrators such as Lockheed and Boeing. Together they should work with the Standards Developing Organizations (SDOs) that shepherd the technology. The DoD needs to assign leaders with the influence to make things happen, who can unify their own internal differences and work with the appropriate industry SDOs to influence them to work collectively. The framework is in place. It's time to solve world interoperability!

For more information, contact Jerry at jgipper@opensystems-publishing.com.

DoDAF: Architecture Development Process

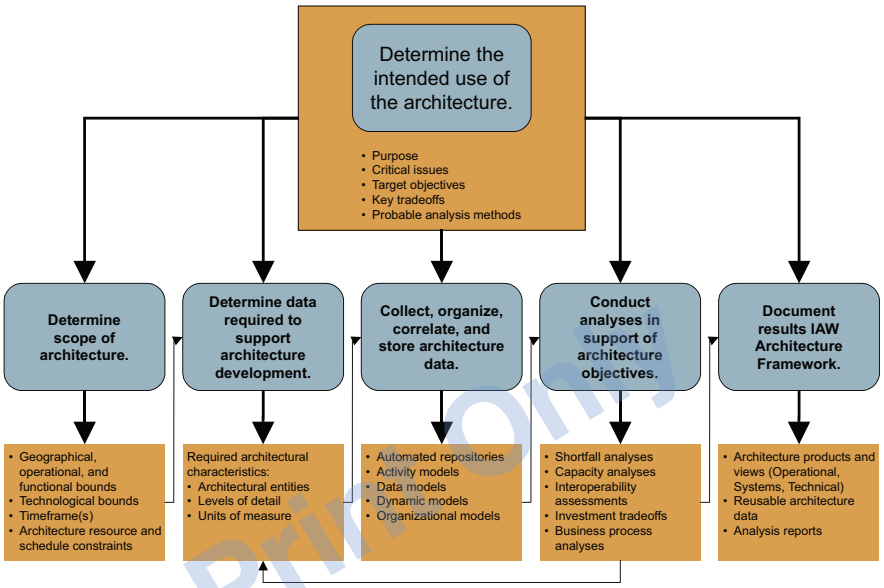
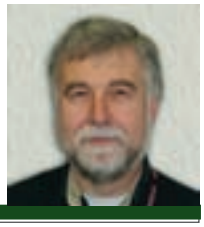


Figure 1

Field Intelligence

By Duncan Young

Filling the gaps in COTS subsystem integration



As the digital battlefield takes shape, it is becoming ever more difficult to define the boundaries and requirements for embedded computing systems. Platforms such as combat aircraft, helicopters, or UAVs – which themselves may contain many tens of subsystems – are required to perform their missions cooperatively with any other types of platforms, adding to overall complexity. COTS suppliers must step up to understand the broader issues of how their products will be used if they are to offer integrated subsystems to their customers.

The RQ-8 Fire Scout UAV, which Northrop Grumman supplies to the Navy, is a good example of such a complex system. The Fire Scout was designed for Vertical Take Off and Landing (VTOL) operation from the helicopter deck of a warship and can carry out much of its mission semiautonomously. Designed initially as an aerial surveillance platform with streaming video feed to the surface, Fire Scout, illustrated in Figure 1, has continued to evolve to accommodate multiple sensor types plus air-to-ground weapons, becoming the RQ-8B. It has now been selected as the Class IV-A brigade-level UAV for the Army's Future Combat System (FCS).

As platforms such as Fire Scout evolve, they take onboard more embedded computing capability. These platforms would typically take the form of enhanced flight management systems, multisensor payload interface subsystems, and enhanced intra-platform networking based on Ethernet or switched fabric technologies. To reduce project costs and time-to-deployment, subsystems such as these are based on COTS modules and software, which also enables rapid prototype assembly and earlier integration. To consolidate these benefits and capitalize on their extensive product knowledge, COTS suppliers may be tempted to offer integrated, application-ready subsystems for this class of project without a deep enough appreciation of the complexities involved.

Successful COTS subsystem specifications will include these application-level requirements:

- Multilevel I/O and networking interoperability – physical, electrical, protocol performance and response, and driver requirements
- Processor performance, memory capacity, and bandwidth available for the user's application above RTOS, drivers, and middleware
- Response of processor/RTOS combination to external stimuli
- Critical algorithmic performance parameters

Figure 1. Northrop Grumman RQ-8 Fire Scout UAV

To many, a COTS subsystem would be adequately described by its I/O ports, memory size, memory bandwidth, procesor performance, and support for an off-the-shelf RTOS. However, these are only a fraction of the parameters that might need to be specified to fit a new subsystem into the aforementioned UAV example. Interoperability among the new subsystem's individual components should be a given, but how should subsystem interoperability with the remainder of the existing platform be defined? A supplier's I/O device driver might be optimized for interrupt-driven operation only, yet the subsystem might have real-time response or determinism requirements that preclude using interrupts. Another example may be the performance of an IP stack that adversely affects communications between already tested and proven subsystems within the platform. These types of issues require more than a tick in the box during the selection process.

To be succesful in the subsystem integration business, COTS vendors must invest in ways to better understand their customers' needs. It will be necessary to develop domain expertise – people with application knowledge of control laws, radar, sonar, graphics, safety criticality, determinism, networking, and communications, as well as the traditional specialist product knowledge. It will be necessary to offer advice and preempt potential problem areas with workarounds or modifications to standard products. Very often, the solution will be to offer alternative configurations to overcome potential performance shortcomings. The ideal is to offer proof through benchmarking or prototyping in a representative platform environment before the configuration is cast in stone.

Figures 2 and 3 illustrate equipment based on COTS integrated subsystems from GE Fanuc that have been successfully deployed on UAV platforms, including Fire Scout. These are fully enclosed with their own power supplies and have been qualified to meet the requirements of MIL-STD-810. Figure 2 shows a 3U CompactPCI mission computer. The rugged RES-110 Ethernet switch illustrated in Figure 3 is designed as an intraplatform managed Layers 2 and 3 GbE switch. Based on off-the-shelf subsystems, the final configurations of these subsystems as delivered to the customer demonstrate the value of open dialog during the selection and prototyping phases of project development.

Figure 2

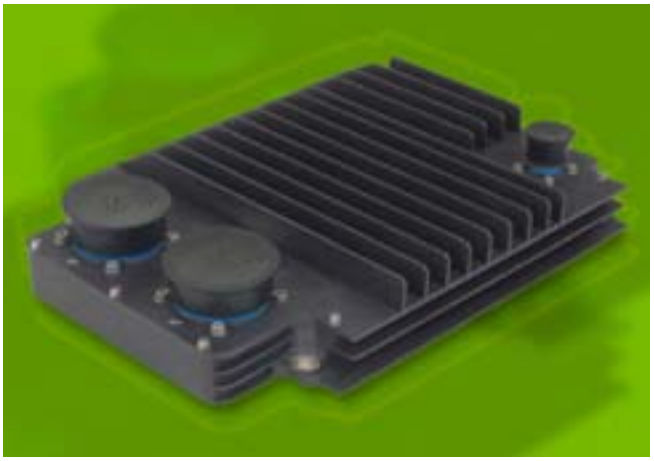


Figure 3

Even 12 years from the introduction of COTS as mandated procurement policy, there are still best practices to be explored and lessons to be learned, particularly in the case of subsystem integration. The rapid pace of technology growth that has transformed the war fighting capability of today's military systems may have created a requirements analysis gap in its wake that only COTS suppliers themselves can fill. Recent industry consolidations now give the major players the muscle to successfully fill this gap and realize the market potential of integrating COTS subsystems. The solutions are likely to be found in the right blend of domain experts, benchmarking, performance specification in application-like environments, and new, layered interoperability models that could become part of a common equipment specification language. This can only help fuel greater COTS adoption and close the gap between contractors' and suppliers' needs and expectations.

To learn more, e-mail Duncan at young.duncan1@btinternet.com.

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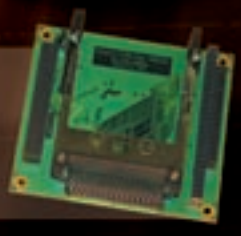

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Letter to the Editor

Dear Editor,

In the Fall 2006 *Military Embedded Systems* article *The COTS software market doesn't run on DOD time*, you wrote that "One only has to look at defunct languages such as Forth or the barely commercially viable Ada environment to understand that the military has little or no clout with the COTS software industry."

We at AdaCore respectfully disagree with the statement that Ada is "barely commercially viable."

AdaCore, whose sole business is the support of the Ada programming language and Ada programmers, has shown steady growth and profitability since its inception in 1994 with an average growth rate of nearly 30 percent per year, and an impressive list of Ada programming customers. Not only has our support for legacy, current, and future Ada development needs (Ada83, Ada95, and the new Ada2005) built a successful business model for AdaCore, but use of the Ada language itself has continued to grow in those areas where the language provides its greatest benefits. This is most notably the safety- and security-critical software marketplace where Ada's strong typing, compile time error checking, runtime checks, and built-in exception handling, among other features, allow for the development of systems that are more reliable and thus more readily meet safety and security requirements. In today's safety- and security-conscious world, we feel this market will only continue to grow.

Another tangible indicator of Ada's viability is the success AdaCore's GNAT Academic Program (GAP). Dedicated to building a community of academic Ada professionals, GAP grew to more than 100 institutional members less than a year after the initiative was launched. Through GAP, new Ada programmers are being trained and launched into the marketplace.

The Ada market is healthy: According to an industry survey sponsored by the Ada Resource Association (ARA), the total costs of systems in which Ada plays a critical part is at least $5.6 billion in Europe and North America. The ARA, an international nonprofit organization, maintains the Ada Information Clearinghouse and comprises principal suppliers of Ada development environments and tools: AdaCore, IBM Rational Software, Praxis Critical Systems, and SofCheck.

The full report is posted on the ARA website at:
http://www.adaic.com/news/survey-results.html

Interestingly enough, AdaCore's supported product lines very much follow the model presented in the follow-on article titled: *The emerging practice of software product line development*. AdaCore develops and supports Ada compile systems. These must be planned from the start to support a variety of host platforms, then both native and cross-embedded targets. The product lines are developed with reusable and portable front-end components. These are designed to be easily ported to the multitude of native host platforms we support. Target-specific native or embedded components or back-ends are then plugged into this front-end technology to provide technologies such as target-specific code generation. This is perhaps a simplified description of our software development model, but one shared by many vendors that support compile systems. We fully agree with the author's conclusion on the advantages of this approach.

Sincerely,
Greg Gicca
AdaCore
Director of Safety and Security Product Marketing

Part 1: Design and implementation of an SCA core framework for a DSP platform

By Carlos R. Aguayo Gonzalez, Francisco M. Portelinha, and Jeffrey H. Reed

(This article is based on a paper presented at the SDR Forum Technical Conference November 2006, Orlando, Florida.)

Editor's note: This is Part 1 of a two-part article. Part 2 will run in the next issue of Military Embedded Systems.

The authors present the design and implementation of the SCA 2.2 Core Framework for a TI DSP platform and provide the rationale behind design decisions and initial profiling results.

The Software Communications Architecture (SCA) was developed by the Joint Tactical Radio System (JTRS) program of the U.S. Department of Defense (DoD) to standardize the development of Software-Defined Radio (SDR) technology. The SCA was developed to enhance system flexibility and interoperability, while reducing development and deployment costs. As with most emerging technologies, early implementations of SCA SDRs have struggled to meet performance, cost, size, and power requirements. Arguably, many of these struggles have their origin in the assumption of a modular, distributed platform based on General Purpose Processors (GPPs) performing all signal processing.

Traditionally, developers have relied on Moore's law to overcome processing power shortcomings. However, in order to deal with the challenges of implementing SDRs, it is necessary to use technology as efficiently as possible. DSPs, for instance, are specialized microprocessors designed specifically for real-time digital signal processing. They have been used for decades in the communications industry to implement radios in resource-constrained environments. In spite of this, DSPs have been relegated as secondary elements in the SCA, requiring a Hardware Abstraction Layer (HAL) for connectivity. Ongoing improvements in development tools and middleware have leveraged DSP technology to fully support the SCA. By following this approach, the flexibility and reusability brought by the SCA are complemented by the cost and power efficiency of DSPs. If taken to a logical extent, this approach could eliminate the need for a GPP on certain SDR implementations.

System architecture

Our system's general software structure is shown in Figure 1, where three different components of the SCA Operational Environment (OE) are shown: Core Framework (CF), CORBA middleware, and Operating System (OS). The last element of the SCA OE, Services (for example, Log, Event, and Naming Services), was not considered for the initial implementation. The Open-Source SCA Implementation Embedded (OSSIE)[1], developed by Wireless@Virginia Tech, Mobile and Portable Radio Research Group (MPRG), was used as the CF.

The ORB used in this project is PrismTech's e*ORB SDR C++ version for DSP[2]. This is an optimized, modular implementation of Minimum CORBA as standardized by the Object Management Group (OMG). e*ORB also supports the Extensible Transport Framework (ETF), which allows custom transport plug-ins.

DSP/BIOS was selected as the OS. It is a scalable real-time multitasking operating system designed specifically for the

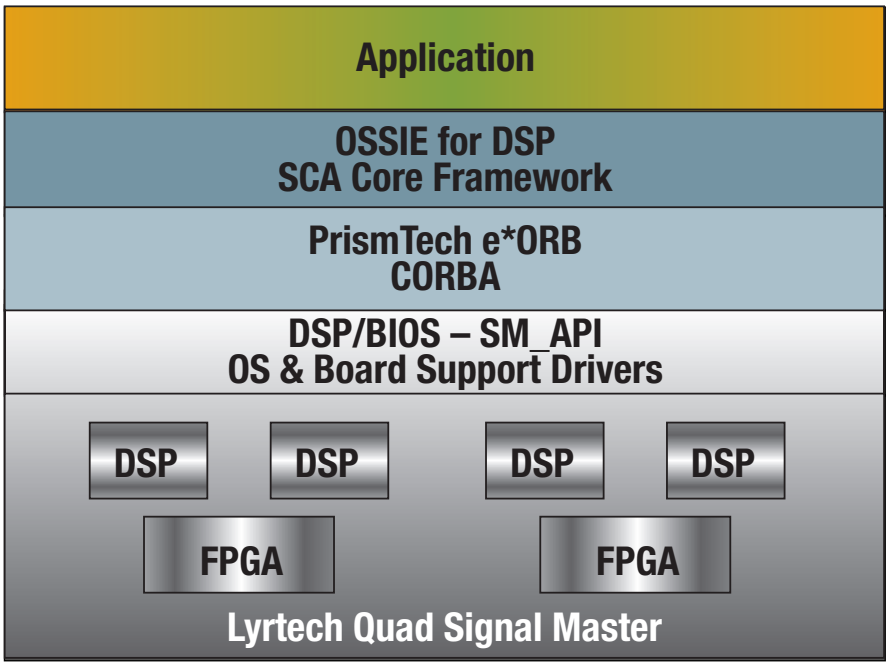

Figure 1

TMS320 family of DSPs[3]. It supports preemptive multithreaded operations because of a real-time scheduler, and provides memory management modules for low overhead, dynamic memory allocation. Note that DSP/BIOS is not POSIX compliant, as required by the SCA.

The target hardware platform for this project was Lyrtech's SignalMaster Quad C6416[4]. This high-performance board contains four TI TMS320C6416T DSPs and two Xilinx Virtex-II FPGAs divided into two clusters (one FPGA and two DSPs each). The system runs at 720 MHz and has 128 MB of SDRAM memory per DSP. There is a high-speed bus between both FPGAs implemented using LVDS. The communication between two DSPs within the same cluster can be implemented using shared memory or FastBus, a proprietary protocol developed by Lyrtech. Only DSPs were used for signal processing and framework functionality. FPGA operation was limited to inter-DSP communications.

OSSIE C64 implementation

The key task for the success of this project was porting the C64 platform of the original version of OSSIE, which runs on an x86 platform running Linux and uses omniORB as middleware. The development platform was Code Composer Studio (CCS), an integrated development environment for TI DSPs, with version 5.1.0 of its Code Generation Tools. This particular version lacks the Standard Template Library (STL) and has limited support for C++ exceptions. In the absence of exception support, we used CORBA Environment variables coupled with a set of macros, distributed as part of e*ORB, for error handling.

A very important aspect to consider is the absence of a Memory Management Unit (MMU) in the C64. The MMU is responsible for handling memory access requests. It takes care of virtual memory management, paging, memory protection, and bus arbitration. Its job is to take pieces of dispersed physical memory and present them to the requesting process as a contiguous block. As a result of using a MMU-less platform, all memory management is the responsibility of the developer. Certain OS calls, such as fork(), are not supported.

Another important development area was porting all scheduling calls to the preemptive, multithreaded DSP/BIOS. The main difference from a traditional fair-share OS is that the active task with the highest priority will be scheduled for execution, no matter how many other tasks are waiting, or for how long. This characteristic allows deterministic execution, crucial in real-time systems, but makes the developer completely responsible for task scheduling and priority assignment.

The SCA specification requires the reading of the XML Domain Profile at runtime to obtain deployment and configuration information (for example, the implementation of ApplicationFactory must read a Software Assembly Descriptor file in order to know which components are included in a given waveform and respective connections). Parsing XML is a complicated task for a DSP, and there are not many tools available to help with it. To facilitate development, reduce memory requirements, and speed execution, a two-step parsing scheme was implemented. In this scheme, shown in Figure 2, an offline translation of the XML files into a simplified format was performed. This two-step parsing did not affect the traditional SCA waveform design cycle and only added one extra step at installation time. The savings in time and complexity, along with the uncompromised portability of the resulting waveforms, justified this decision.

Because our hardware platform did not have long-term storage capability, only a partial implementation of a file system was developed. The host computer's hard drive and file system were used to store the translated domain profile files. Due to limited I/O functionality in the runtime support library, directory-related interfaces (such as mkdir, rmdir, mount, and unmount) were not implemented.

The SCA specifies two equivalent mechanisms to launch software components: ResourceFactory and ExecutableDevice. In our design, the former was used to launch components in the host node (the one that loaded DomainManager), and the latter was reserved for remote nodes and required a DeviceManager. Due to the absence of a transport layer, only ResourceFactory was implemented. This was done using DSP/BIOS scheduler, with a new task being scheduled every time a new component instance was required. This behavior requires that all software tasks are loaded in program memory before they can be scheduled. ResourceFactory was in charge of managing the new task's priority.

Sample application

Framework functionality was demonstrated by deploying two sample applications. These applications were intended for demonstration purposes and nothing else. No extensive signal processing was performed. The main goal for these applications was to verify framework operation and corroborate the feasibility of deploying SCA-compliant waveforms onto the C64 platform.

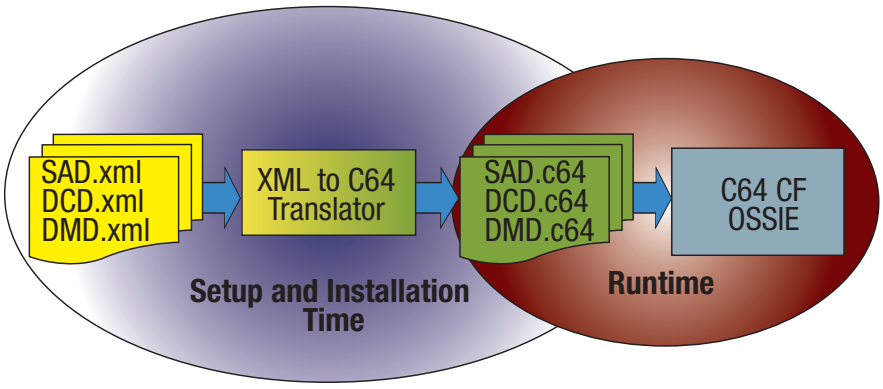

Figure 2

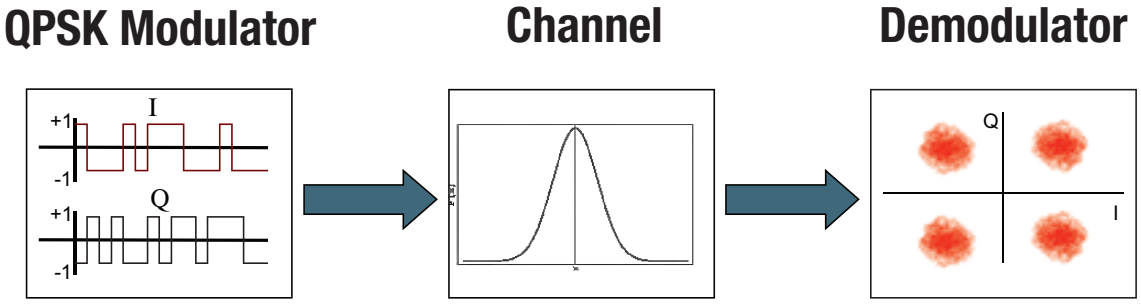

Figure 3

The first application includes three simple components: Binary Phase-Shift Keying (BPSK) modulator, channel, and demodulator. The BPSK modulator generates a random stream of 1s and -1s. The stream is passed to the channel component, which adds Gaussian noise to the in-phase and quadrature components of the stream. The demodulator only displays the constellation diagram of the signal. The second waveform includes a Quadrature Phase-Shift Keying (QPSK) modulator instead of BPSK. Figure 3 shows a graphical representation of the second waveform. Both waveforms were successfully deployed on a single-chip configuration using the ResourceFactory interface to launch the components.

Acknowledgments

This work was supported by Texas Instruments, PrismTech, Mercury Computer Systems, Lyrtech, and the National Institute of Justice.

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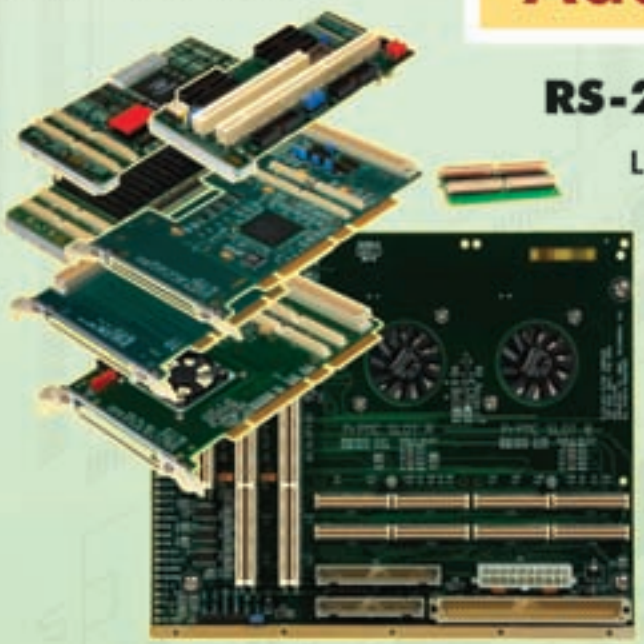

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Understanding neutron single-event phenomena in FPGAs

By Joe Fabula, Jason Moore, and Andrew Ware

Aerospace and defense programs drive some of the most challenging requirements. Long program lifetimes and stringent reliability add to complex trade-offs between performance, cost, and program schedule. Reconfigurable FPGAs are increasingly enabling these markets. Xilinx and other vendors provide long product life-cycle support as well as radiation-tolerant silicon and packaging. In addition, new FPGA capabilities such as embedded microprocessors and DSP are augmenting the reconfigurable FPGA's inherent flexibility. One key design requirement revolves around high-assurance systems subject to atmospheric Neutron Single Event Upset (NSEU) radiation effects. A lack of consistent NSEU data combined with an abundance of opinions have clouded the true FPGA market requirement.

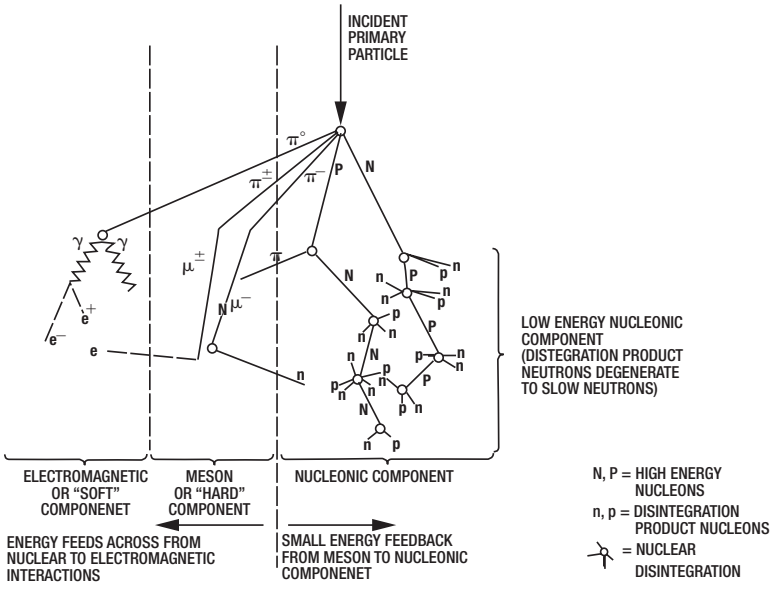
Experimentally measuring the NSEU sensitivity of any IC is a challenging task due to the low atmospheric neutron flux rates (even at elevated altitudes), the non-ideal flux-energy distributions found in highly accelerated neutron beam sources, and the small sample sizes available for testing. In addition, limited in-system test capability with some IC vendors makes data collection difficult or impossible. The designer requires NSEU data and an understanding of the system and environmental requirements in order to properly design an application to meet system reliability and availability specifications. The responsibility falls to the IC manufacturer to provide the designer the information required to properly evaluate a high-assurance system's response to atmospheric radiation.

NSEU tolerance is not just an FPGA issue. State logic such as flip-flops and embedded memory in any generic IC is also susceptible to atmospheric radiation. While in many cases the IC state logic can be and often is more susceptible than an FPGA configuration memory cell, we will focus on the latter case only.

Xilinx has been studying NSEU and other radiation effects for a decade. It continues to perform extensive accelerated testing at the Los Alamos Neutron Science Center (LANSCE), as well as real-world NSEU testing at different altitudes and latitudes around the world. The latter test program is used to bridge the gap between accelerated testing and real-world results. After gathering and publishing thousands of device years' worth of real-world test data, the conclusions are clear: Real-world testing is critical to demystifying NSEU effects, and reconfigurable FPGAs can meet the reliability targets demanded by the aerospace and defense market.

NSEUs and NSEU data collection

Atmospheric neutrons are residues of space – heavy ions – and solar particles like high-energy protons and coronal mass ejections, which impact the upper atmospheric nitrogen and oxygen atoms. These interactions create a collision cascade of particles, some of which are long lived and find their way down to the surface of the Earth. When they reach Earth, this cascade of particles is composed primarily of high-energy neutrons plus a small altitude-dependent percentage of protons (Figure 1). These neutrons will interact with matter. A neutron interacting with a silicon nucleus can create alpha particles and other charged nuclei that create a charge tail.



Schematic Diagram of Cosmic Ray Shower

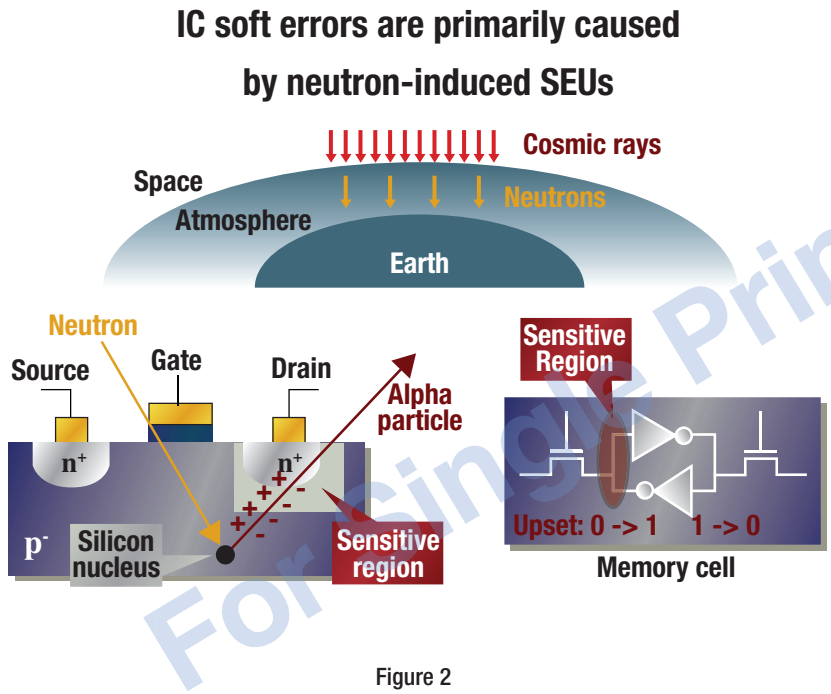
- High-energy (>> GeV) primary particles from the cosmos don't make it to terrestrial levels (~0 to 10 kFT)
- High energy neutrons:
  - > Make it through the atmosphere to terrestrial levels in significant numbers
  - > Can penetrate semiconductor packaging
  - > Have some finite scattering cross section (that is, can cause upset)

Figure 1

If strong enough, the charge tail may flip a bit or change state in an SRAM memory, a latch, or FPGA configuration cell. This upset is called an *NSEU* or *soft error,* since no permanent damage is done to the latch. Depending on the function being performed, the NSEU may affect the functional output of the device in the case of an upset configuration cell (Figure 2).

A seemingly trivial question is: What is the total neutron flux and flux rate that an FPGA designer must account for when designing a system to meet specific customer requirements? In a *study of studies* on the experimental measurement of neutron flux and energy, Ziegler[1] showed that previous results varied widely and can lead to errors of as much as 10 to 1 in neutron flux and/or neutron energy profiles at any specific site, depending on the data set chosen (Figure 3). With a 10 to 1 error, you could basically pick any answer you wanted.

This wide range of data introduces uncertainty in the neutron flux and/or neutron energy that must be accounted for in the design effort. The engineering team ultimately will be held accountable for the long-term success of their program and can't afford to design to speculation. Rather, they must design to meet hard system reliability and availability specifications, as well as to support their design choices with reliable, accurate neutron sensitivity data.



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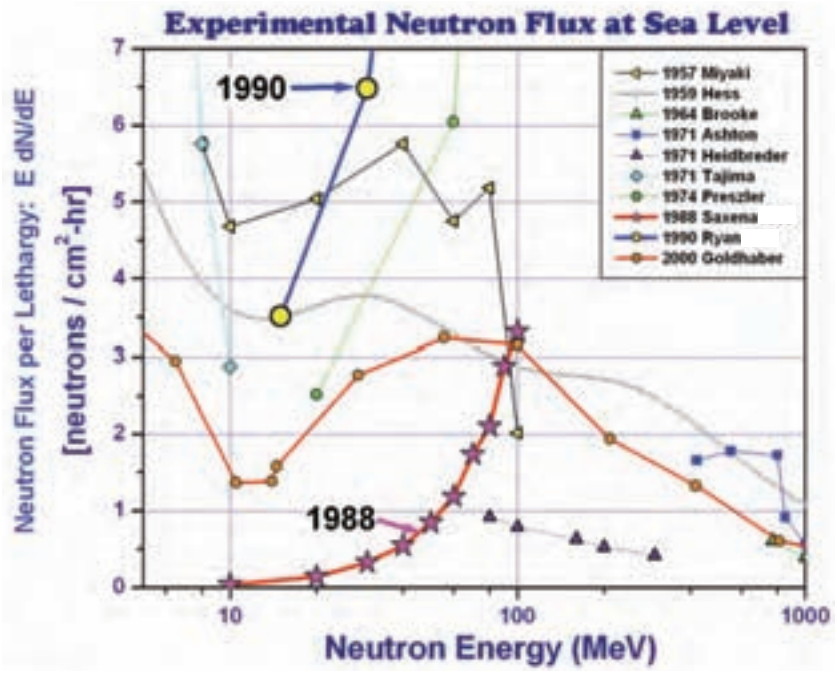


Figure 3

Understanding the necessary terminology

When further delving into the details of neutron single-event phenomena in FPGAs, it's important to first understand some basic definitions. They are:

- **Soft error:** An NSEU-induced bit-flip in the configuration memory. Soft errors may or may not induce a functional error and are correctable with no permanent damage to the cell, hence the term *soft.*
- **User Logic Upset Rate (functional failure):** Incorrect design behavior caused by a soft error in a critical configuration memory cell.
- **SEU Probability Index (SEUPI):** The ratio between the soft error rate and the functional failure rate. In Xilinx devices, for example, the SEUPI value is conservatively estimated at 10:1. This means that a designer can expect one functional failure for every 10 soft errors.
- **Single Event Functional Interrupt (SEFI):** A functional error that requires FPGA reconfiguration or power cycle to erase the error.

It should be noted that soft errors and SEFIs are often mixed up in literature. In fact, soft errors are not equivalent to SEFIs, or even to logic upsets.

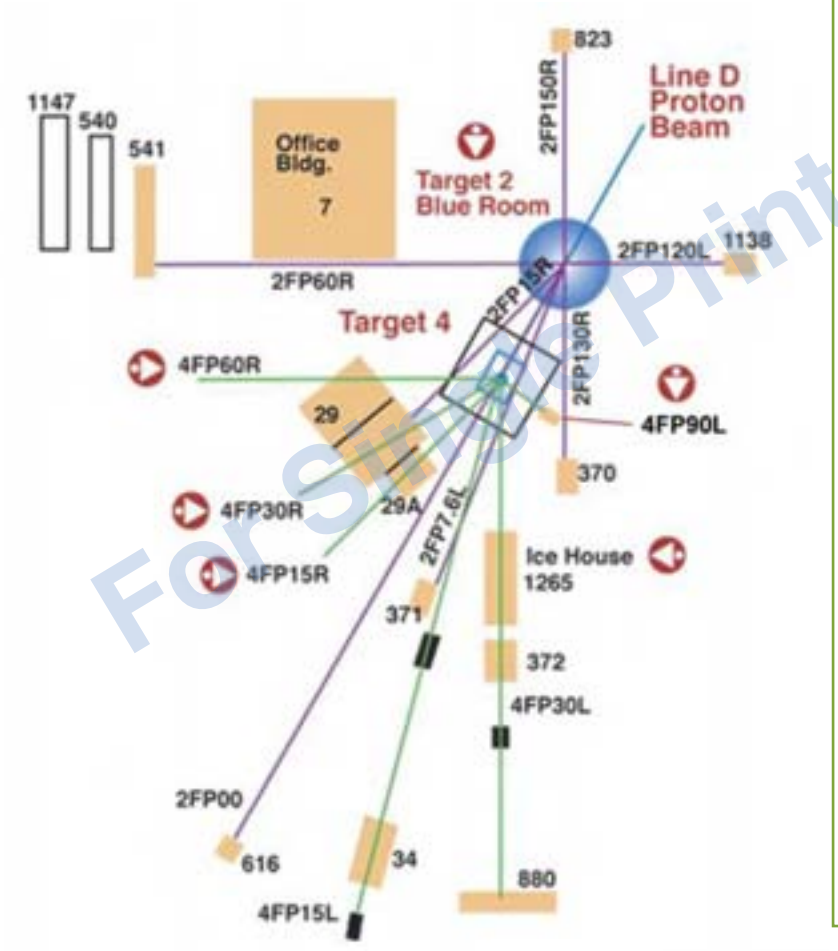
Accelerated neutron beam testing of FPGAs is one useful way to approximate reality. An example is the neutron beam at the Los Alamos Neutron Science Center. Its beam profile is a reasonable fit to theoretical atmospheric neutron profiles, but at much higher flux. This higher flux enables much faster testing than a real-world test, which would require multiple years or large numbers of devices (Figure 4).

While accelerated neutron beam testing may point the engineering team in the right direction, correlating those accelerated testing results to real-world performance of hundreds of parts over many months or years, at multiple locations (altitudes and latitudes), is required. In addition, accelerated testing typically involves exposing at least a few devices to an artifact (the beam) that simulates and accelerates, but which does not really recreate the natural environment. Another drawback is that the beam is just a *reasonable* fit – off by 3x at lower energies (refer to Figure 4). Also, experimental results can vary over each run; we have seen variations up to ± 20 percent.

Real-world data

To account for these variations, Xilinx embarked on a program called *Rosetta*[2] four years ago that measures real-world NSEU effects in FPGAs. Hundreds of devices are being monitored for NSEU effects at several diverse atmospheric locations such as Albuquerque, New Mexico (5,100 feet), San Jose, California (0 feet altitude), White Mountain, California (12,500 feet), Toulouse, France (472 feet), Plateau de Bare, France (8,171 feet), Mauna Kea, Hawaii (13,200 feet), and in a nuclear storage bunker 1,500 feet below ground level in Toulouse, France. Figures 5 and 6 show the inside and outside of the White Mountain facility.

In total, Rosetta has obtained more than 220,000 Mbit-years' worth of testing over multiple process geometries. Further testing is ongoing. An *Mbit-year* is defined as 1 Mbit worth of configuration data testing over the span of one year. Xilinx realized 1,700 device hours of testing in the LANSCE beam last year alone. Multiplied by the acceleration factor of 10^5 (the factor of beam neutrons over normal sea-level atmospheric neutrons), this corresponds to 335,000 Mbit-years of beam testing. This amount of testing is orders of magnitude more than typical program lifetimes.



Neutron exposures are performed at the ICE house (Integrated Circuit Exposure facility) where a neutron beam with an energy distribution similar to the atmospheric neutronflux at 40,000 ft is available.

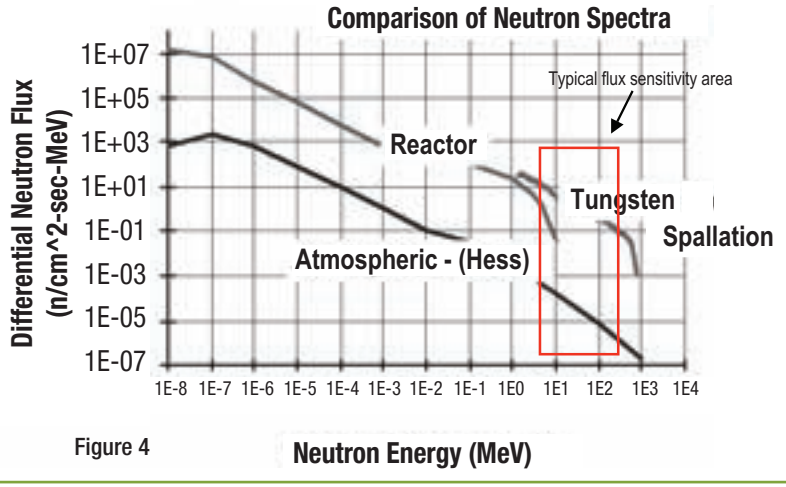


Figure 4

Figure 5

Figure 6

The results of both test methods are detailed in Table 1. Note that both FPGA configuration bit upsets and any Single Event Functional Interrupts (SEFIs) were monitored. To date, no SEFIs have occurred in the Rosetta testing. The cross-section is the altitude independent, normalized measure of device NSEU susceptibility.

Converting the cross-section to Failure in Time (FIT)/Mb can be accomplished via the following equation: FIT/Mb = Cross-section*14.4*10^9*10^6, where 10^9 is the FIT definition (1 FIT is per billion hours), 10^6 is to normalize per Mbit (10^6 bits) of configuration data, and 14.4 is the sea level neutron flux per square centimeter-hr.

The data is striking. One would assume that shrinking IC process geometries would imply worsening NSEU tolerance, as is feared – and has been actually seen – in some commercial SRAMs. The charge storage at a 90-nm gate is smaller than at 130 nm, meaning there should be less charge (created by a neutron spallation reactions) required to upset those bits. Yet the shrinking cross-section and lower failure in time or FIT rate show otherwise. Note that NSEU tolerance in Xilinx designs also has improved for new designs within each process node over time since the 220 nm node.

The high-performance, feature-rich FPGA configuration cells that Xilinx uses are sometimes confused with simple SRAMs. Xilinx designs its static-latch configuration cell to a different standard than SRAMs. This data shows that the static-latch design has not only stabilized but improved both over earlier process nodes as well as within process nodes. Xilinx also designs its lookup table logic to the same standards of reliability.

Process Node	Rosetta Mbit-years test time	Accelerated test config. bit cross-section (10 MeV model)	Rosetta Config. bit cross-section (sea level FIT/Mb rate)
150 nm (Virtex-II)	120,000	2.4E-14	2.8E-14 (400 FIT/Mb)
130 nm (Virtex-II Pro)	68,000	2.6E-14	2.7E-14 (390 FIT/Mb)
Gen I 90 nm (Spartan)	1,300	2.2E-14	1.2E-14 (170 FIT/Mb)
Gen II 90 nm (Virtex-4)	33,000	1.8E-14	0.33E-14 (48 FIT/Mb)
Gen III 90 nm (Spartan 3E)	*	1.4E-14	*More test time required for statistical significance

Table 1

Based on the results of this testing, Xilinx correlated the real world to the accelerated testing data sets of its products. It determined the correct neutron energy model (>10 MeV) that correlates with the real world to use when calculating upset rates using accelerated testing data. Based on this corrected energy model, it was determined that FPGAs in the real world are less susceptible to NSEU effects than predicted by accelerated testing by around a factor of up to 5 times, especially at smaller process nodes. Note, therefore, it is incorrect to extrapolate the 1.5-MeV model, which is often used in SRAM data calculations and many FPGA procurement specifications.

Real-world data now enables faster time to evaluate FPGA designs in an accelerated beam, more accurately correlating accelerated beam data to what can be expected in the real world. These experiments also show the importance of Rosetta-like experiments for any accelerated tests on an FPGA or an IC such as an ASIC.

Is the NSEU a functional error?

The SEU Probability Index (SEUPI) is the ratio between configuration bit upsets and functional failures (user logic upsets). Many Xilinx customers have performed their own studies and shown that the ratio

of NSEUs to logic upsets can be as high as 25 to 100 times. Stated differently, an accumulation of 25 to 100 configuration cell soft errors is typically required to cause a functional failure. A conservative rule of thumb is that since at most ~10 percent of the configuration cells – even in a dense design – are used in a typical FPGA design, the ratio of soft errors to logic upsets is at least 10 to 1. The logic upset rate of an FPGA is very small compared to the configuration cell upset rate.

True upset rates can now be calculated to show the insensitivity of static-latch FPGAs to NSEUs. As previously mentioned, *cross-section* is defined as the common measure of NSEU upset rates – the probability that a single neutron flips a single bit. Given that, Mean Time to Functional Failure (MTTFF) can be calculated as follows:

Sea Level MTTFF (hours) =
SEUPI * [1/(Configuration Bits*Neutron Cross Section*14.4)]
or
Sea Level MTTFF (hours) =
SEUPI * [10^9/(Mb of Configuration Bits*FIT/Mb rate)]

Hours can then be converted to years by the standard 24 hours/day *365 days/year factor. In Table 2, altitude multiplying (reduction) factors are calculated using the JEDEC standard number JESD89 above the Sea Level value of 14.4 (a 9.73 reduction factor at 10,000 feet).

Note that while the largest, most dense Virtex-4 devices can have on the order of 51 Mbits of configuration data, the factor of a 3.5 reduction is still a large MTTFF. There are also factors such as latitude and even sunspots that add some additional bound on these numbers; both those effects aren't large enough in aggregate to impact these conclusions. In fact, the table is conservative given the low choice of the SEUPI factor of 10.

Real-world results are the key

Although there will always be application-dependant choices in design, a couple of threads are common to these design problems in achieving NSEU tolerance. First, it is critical to use the correct neutron models. Second, while accelerated testing helps shorten the time it takes to evaluate NSEU effects, this testing must be correlated to real-world results to ensure that accurate requirements are obtained.

Xilinx has invested more than 230,000 Mbit-years of real-world testing in dealing with the issue of neutron single-event phenomena. More importantly, it has taken the *known unknown* of NSEUs and quantified it, enabling designers to use reasonable design margins to reach their reliability targets. Armed with this information, reconfigurable FPGAs can be confidently used over less capable technologies.

Joe Fabula *is the senior staff member, radiation effects and operations, at Xilinx. He started his career at RCA and ITT, holding various engineering and later management positions spanning 26 years. He joined Xilinx in 1991 as the director of quality assurance, a*

Device	Altitude	Config. memory size	Rosetta Configuration bit FIT rate (FIT/MBit)	MTTFF including SEUPI correction of 10
4VLX25	0 feet	8 MBit	48	3,000 years
4VLX25	10,000 feet	8 MBit	48	310 years
4VSX35	0 feet	14.5 MBit	48	1,650 years
4VSX35	10,000 feet	14.5 MBit	48	170 years

Table 2

position he held for eight years. He is currently supporting Xilinx terrestrial and deep space radiation testing efforts and providing customer applications and quality support for the aerospace, defense, and automotive products businesses at Xilinx Corporation. He earned a BSEE (with honors) from the Stevens Institute of Technology and an MBA in Management from Fairleigh Dickenson University.

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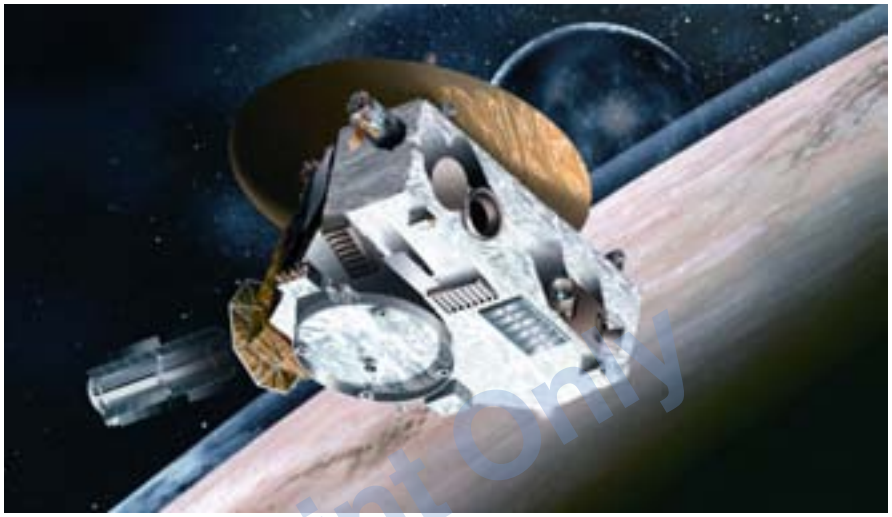
Editor's note: Since this article was written, Xilinx has released the Spartan-3A (S3A) platform (in a 90 nm process) and the Virtex-5 (V5) platform (in a 65 nm process). In both cases, preliminary NSEU data shows improvement over previously released 90 nm products and improvement at the 65 nm process node, which further supports the thesis of this article. Contact Xilinx directly for more information.

Reconfigurable computing platforms:

Adapting for space applications



By Giovanni D'Aliesio

Reconfigurable computing has been an emerging technology, but only recently has the possibility of developing such systems for space become exploited. The idea of reconfigurable computing in space is a hardware designer's dream since the notion of fixing a hardware bug or updating a hardware-implemented algorithm has never been available. Space missions are critical by nature and, therefore, having the option of reconfiguring a system once launched provides numerous advantages and a great deal of flexibility.

Historically, computing engines were designed using a dedicated general purpose processor with software and glue logic in order to achieve the desired function. As both the speed and gate count of FPGAs have increased, computing engines as well as peripherals can be designed directly into these devices. With the possibility of also reprogramming these devices, the notion of creating reconfigurable platforms for onboard processing is of great interest to the space community. The advent of these reconfigurable platforms brings about many advantages and possibilities such as reduced size and complexity, reduced design cycle times, resource sharing, and opportunities for in-space upgrades and repairs. Of course, as with any space design, there are various obstacles to conquer in order to make these systems useable for the space environment. The architecture and methods by which these platforms can be made space-ready will be described herein.

Reconfigurable platforms: Flexibility is key

Long design cycles and high program risk are common in the space industry. This is because once launched, space electronics cannot be repaired; if fixes are possible, they are significantly more expensive than discovering the problem pre-launch. The use of reconfigurable platforms can help reduce the long design cycles and mitigate some of the risk by exploiting its flexibility. Reconfigurable platforms house a reprogrammable FPGA along with supporting circuitry (including other FPGAs). It is the design of this reprogrammable FPGA that does not have to be completed and tested prior to board and unit level integration; it can be done in parallel since the possibility exists throughout the project to update, change, or correct the design. This provides considerable schedule reduction and significantly reduces program risk.

Once a reconfigurable platform has been designed and tested, its reuse on other projects can further reduce design cycle time and risk. Since the fundamental building blocks of the platform have already been tested and verified, the user reprogrammable part can be changed from system to system without having to recheck the entire platform.

Another advantage of reconfigurable platforms is performing upgrades to existing FPGA designs on-orbit. Should a more efficient FPGA design (either smaller or faster) become available post-launch, the system can be upgraded with the newer version. The spacecraft might also encounter a different environment than initially predicted and thus a change in fault tolerance might be required. There might suddenly be a need to exploit triple module redundancy on a particular circuit due to higher radiation levels than expected, such as the increased radiation environment seen by the Galileo satellite when orbiting Jupiter. New orientations or structures being moved around, as commonly occurs on the International Space Station, can point the unit in the sun longer, heating up the circuit and requiring a faster design for the critical application. These situations could never have been easily fixed in the past, but with reconfigurable computing they can now be dealt with as simple upgrades.

The beauty of a reconfigurable system is that the option exists to change either the entire FPGA's contents or a single module within the complete device. For example, if an FPGA is designed to provide JPEG compression as part of its data transfer capabilities, then it is possible to reconfigure only this module should the user wish to take advantage of the JPEG2000 compression algorithm at a later date. Similarly, the device can alternate between functions of low priority that would originally require dedicated real estate, saving space, and potentially the need for another FPGA. A complex set of system calibration functions might only be required when the unit is first powered on; therefore, it can be loaded when required and subsequently removed to free up space to perform other functions during normal operation.

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Architecture

The general architecture of a reconfigurable system has a reprogrammable FPGA at the heart of the design. Radiation-hardened FPGAs are then used to perform mission-critical functions and interfacing as well as performing all the low-level maintenance and verification of the reprogrammable FPGA. These rad-hard FPGAs also maintain and verify other memories within the system. Additional system-specific circuits are usually required and normally interface with the reprogrammable FPGA. A block diagram depicting this general architecture is shown in Figure 1.

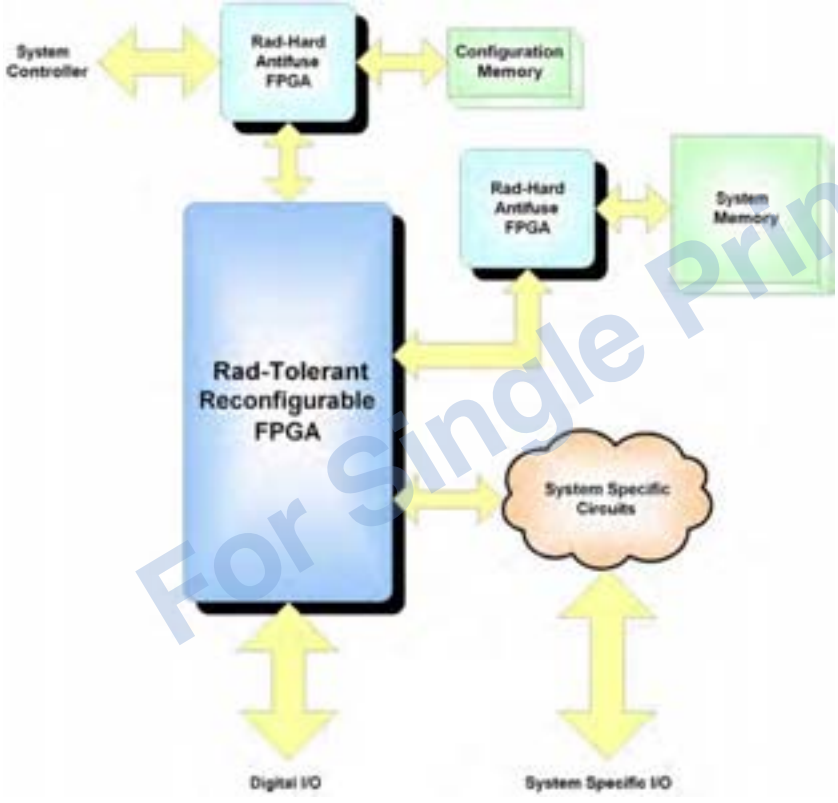

Figure 1

Core functions, which are highly critical to the system, should be kept within the radiation-hardened antifuse Actel FPGA in order to ensure the highest possible immunity to errors. Such functions can be a primary interface to the bus master, reconfiguration, and scrubbing logic, as well as any other mission-specific function that is highly critical. The reconfigurable FPGA, on the other hand, is generally loaded with user code to run higher-level functions and interfaces. Due to their larger I/O capability, they usually interact with the off-chip circuits.

Fault tolerance

Fault tolerance is an important aspect of designing a reconfigurable platform qualified for space use. The effects of radiation in space pose a significant challenge in adapting suitable ground-based designs for use in orbit. Since reconfigurable FPGAs, namely Xilinx's SRAM-based devices, are available as radiation tolerant, they are still susceptible to radiation-induced failures without the proper mitigation techniques. Several techniques are available, a few of which are briefly discussed herein.

TMR

Triple Module Redundancy (TMR) is a method used to enhance reliability by performing a majority vote on three identical circuits. Essentially, the TMR process performs a vote in order to eliminate a potentially erroneous output, thus providing a correct single value. There are several variations of TMR, each with pros and cons, and determining which method is applicable depends on the specific mission requirements.

One method is to use the Xilinx XTMR tool for logic triplication. Since this is an automated process, the main benefit is in its simplicity to implement; however, the inputs and outputs of the device are also triplicated using this tool, reducing the available I/O count by three. Using three physical devices and performing TMR externally in an Actel FPGA is also an option; however, board real estate and power consumption are usually at a premium. TMR can also be selectively used on critical modules only, reducing the amount of triplication required. As an extension to TMR, the voting logic can initiate a scrubbing cycle as will be discussed.

Scrubbing

Scrubbing is a method by which the FPGA undergoes a partial reconfiguration at a constant interval (scrub rate) in order to minimize the probability of observing the effects of a Single Event Upset (SEU). SEU is a radiation-induced error that normally causes a bit flip in memory-based devices. By constantly reprogramming or "refreshing" the contents of the memory, the device is essentially getting a fresh start, removing any bit flips that may have been present.

To determine the frequency at which to perform scrubbing, several factors need to be taken into consideration. The expected upset rate for the given environment is the first indication as to what the scrub interval should be. In fact, it is normally more frequent than the expected upset rate, generally an order of magnitude higher. For example, if the expected upset rate is assumed to be once per hour, then the scrub rate should be once every six minutes. Subsequently, the criticality of the system needs to be known. If the function being performed is of low importance or errors can be tolerated to a certain extent, then scrubbing can be performed at a lower frequency. An equally important factor is the loading of the device. If the system is constantly in use, downtime to perform reprogramming might not be tolerable. In this circumstance, a trade-off needs to be performed to balance system performance and acceptability of errors. This is especially important since the shorter the scrubbing interval, the more reliable the system becomes.

EDAC

Error Detection and Correction (EDAC) is another important aspect in building up the system's fault tolerance. EDAC should be implemented on external memories in order to detect and correct any single-bit errors as well as detect multi-bit errors (and depending on the algorithm, possibly correct double-bit errors). This can be achieved via an antifuse FPGA serving as a memory controller with the appropriate EDAC algorithm.

Examples: Distribution of functional modules

In order to solidify the concept of the generic reconfigurable architecture mentioned above, a real example showing the distribution of functional modules will be presented. The space-ready reconfigurable platform available from MDA is a complete solution for onboard processing. It includes an RF or analog front end, along with the reconfigurable board and electronic power conditioners for both boards, all packaged in a space-qualified stackable chassis. The overall block diagram of the platform is shown in Figure 2. The reconfigurable board can be controlled via an external unit, which could be a processor board such as MDA's PowerPC Enhanced Space Processor (ESPxxx) series. It also contains an interface to the RF/analog board and provides its own interface to external modules.

The block diagram of MDA's reconfigurable board is included as Figure 3. As shown, the reprogrammable Xilinx FPGA is at the heart of the reconfigurable board itself. The configuration memory is stored in Xilinx configuration EEPROMs; however, an Actel FPGA acts as an intermediary controller, handling the con-

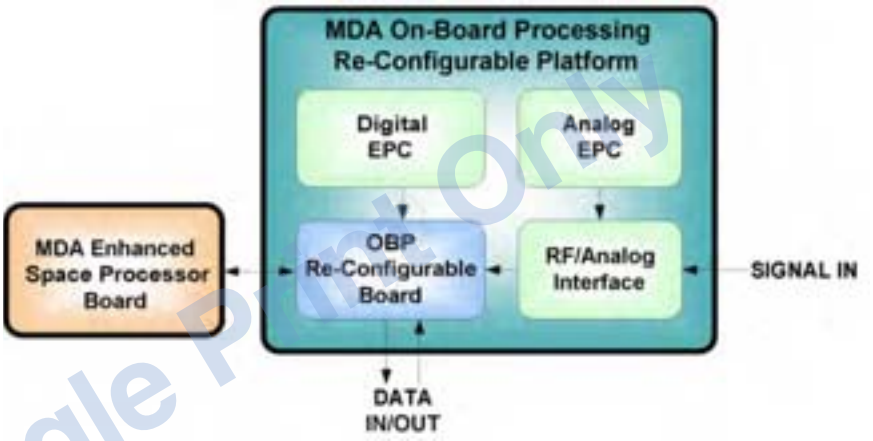

Figure 2

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Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	400	650	400	650	400	650	333	333	333
	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	1	2	1	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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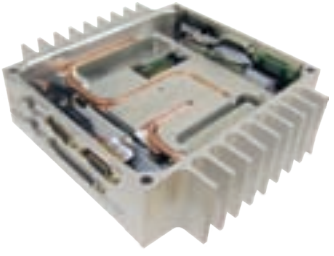

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓
	McBSP Serial Ports	✓	✓				✓							
Analog Input	Single-Ended Inputs	16	16	16	16	16	16							
	Differential Inputs	8	8		8	8	8							
	Max Throughput (kHz)	1250	1250	40	500	100	1250							
	Max Resolution (bits)	12	12	12	12	16	12							
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6							
	Autonomous SmartCal	✓	✓											
	Data Marker Inputs	3	3		3		3							
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k							
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓							
	A/D FIFO Buffer	8k	8k		8k	8k	8k							
	Sample Counter	✓	✓		✓	✓	✓							
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓
	SyncBus	✓	✓				✓							
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48
	Advanced Interrupts	2	2		2	2	2	2	2					2
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M
	Opto-Isolated Inputs										16	48	16	
	Opto-Isolated Outputs										16	16		
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓
	Incr. Encoder/PWM									3/9				
	Relay Outputs												16	
Analog Out	Analog Outputs	2	2		2	2	2	4						
	Max Throughput (kHz)	200	200		200	100	200	200						
	Resolution (bits)	12	12		12	16	12	12						
	Output Ranges	4	4		3	1	4	4						
	D/A FIFO Buffer	8k	8k				8k	8k						

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figuration process as well as the scrubbing activities. This Actel FPGA also provides a CANbus/UART interface to the outside world in order to receive and update the configuration memory as well as provide any status information. A secondary Actel FPGA contains the remaining firmware to be executed by the Xilinx FPGA. The Xilinx FPGA provides LVDS and JTAG interfaces and accepts data from the onboard analog-to-digital converter.

While the use of reconfigurable platforms for space can be extended to almost any application, the following are two examples that are currently in use. The first example is a demodulator in a communications payload, and the other is a data compressor for an onboard scientific instrument, a hyperspectral imager.

The block diagram of the first system (Figure 4) is for a store-and-forward communications payload. A satellite in low Earth orbit is used to gather data from remote locations, such as seismic survey vessels. Typically, data file sizes from such locations are large, in the range of gigabytes, and they need to be transferred to another location in a relatively short period of time.

In this application, the reconfigurable platform contains an RF interface that converts the Cband signal to baseband, which is then sent to the OBP reconfigurable board for processing. Here it is digitized at 525 MSps and then sent to the Xilinx FPGA where DSP algorithms perform demodulation signal processing such as timing synchronization, carrier frequency offset compensation, and phase tracking.

Once the data has been demodulated, the data bits are sent via an LVDS link to a solid-state mass memory capable of storing a terabyte of data. At some later time, when the satellite is over a ground station, the data stored in the solid-state mass memory is retrieved and transmitted to the ground.

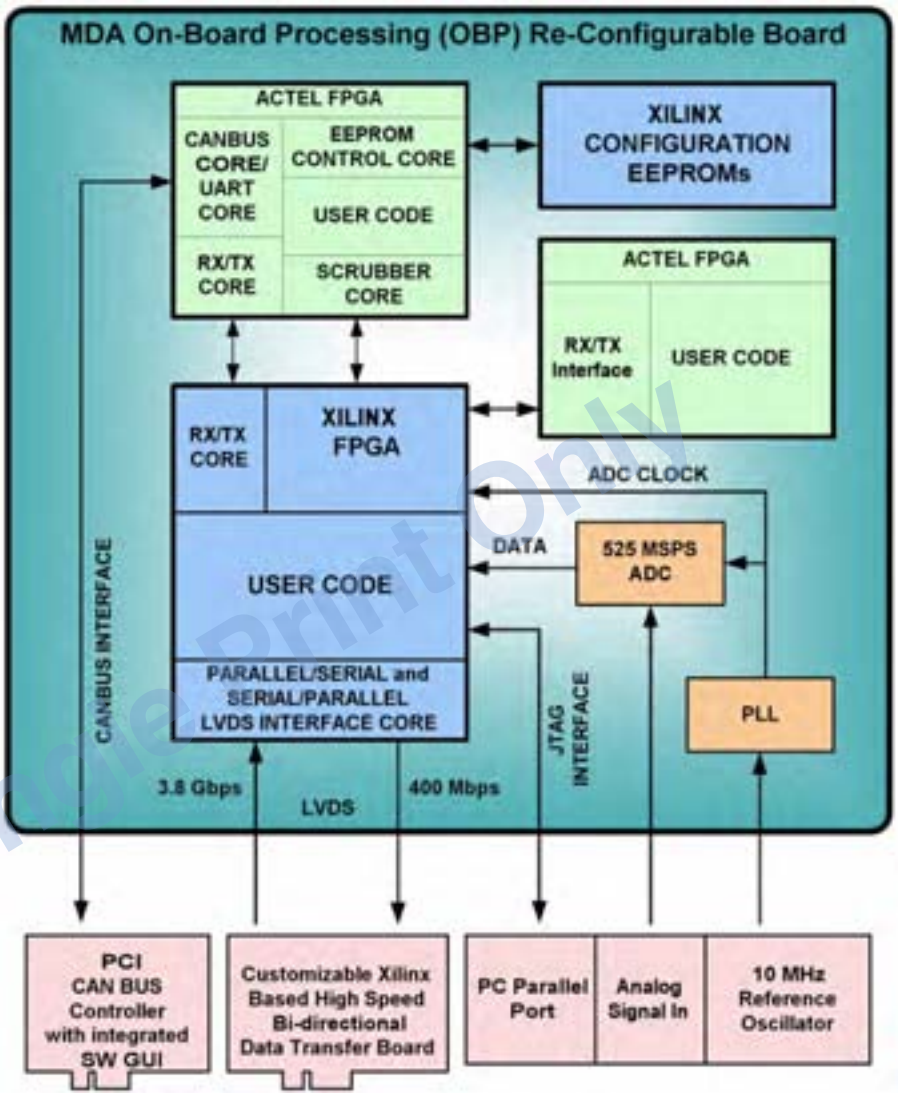

Figure 3

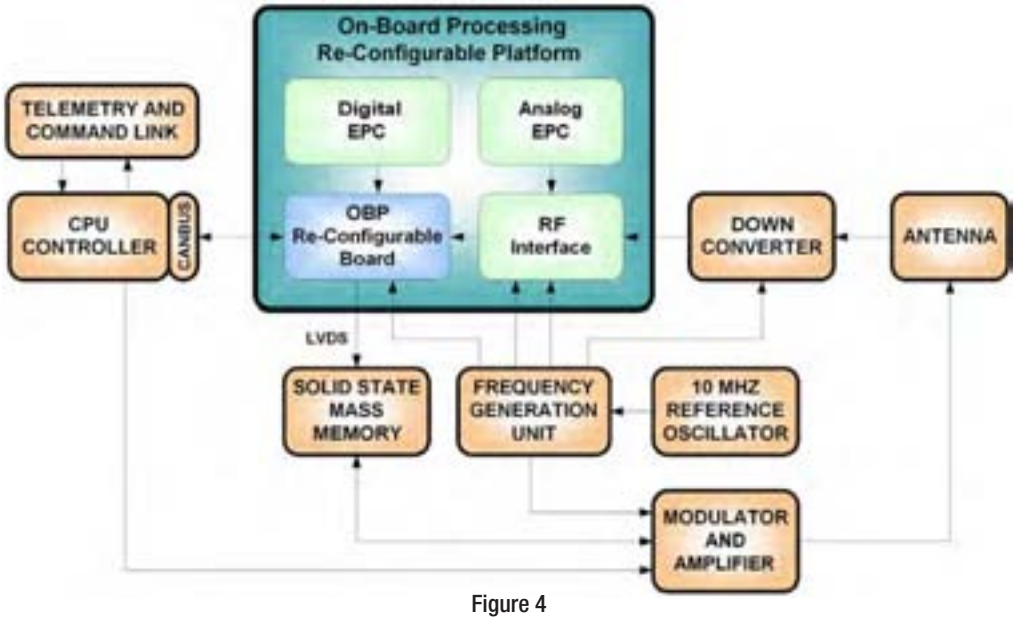

Figure 4

A CPU board communicates with the reconfigurable board over the CANbus, programming its registers when/as needed, and reading the board status information. A low data rate link is used for ground station command and telemetry via a separate antenna. In this application, the reconfigurability of the board can be used to correct certain types of design errors or minor changes in data format.

In the second application, a satellite has a hyperspectral imaging instrument that gathers data from its sensors and transmits the data to the OBP reconfigurable board via an LVDS link. The block diagram of the second example is shown in Figure 5.

In this case, the OBP reconfigurable board implements several algorithms to process the hyperspectral data, one of which is a compression algorithm called *Vector Quantization* (VQ). The VQ algorithm is a complex compression algorithm that requires a large amount of computing horsepower and memory, all of which can be provided by the reprogrammable Xilinx FPGA. The entire VQ algorithm has been designed, coded, tested, and synthesized into the Xilinx FPGA onboard the OBP reconfigurable platform, running at a speed of 100 MHz. It is proven capable of compressing a representative stream of 120 Mbps in real time at a compression ratio of about 16:1 with a reconstructed fidelity approaching 60 dB.

In this application, the reconfigurability of the board is very much an asset. As the signal processing algorithms are modified and improved over time, new images of the Xilinx FPGA can be uploaded. Once again, a CPU board communicates with the reconfigurable board over the CANbus, programming its registers when/as needed, and reading the board status information. The compressed data is transferred to an external memory array via the LVDS link, where it is later retrieved and retransmitted to the ground station.

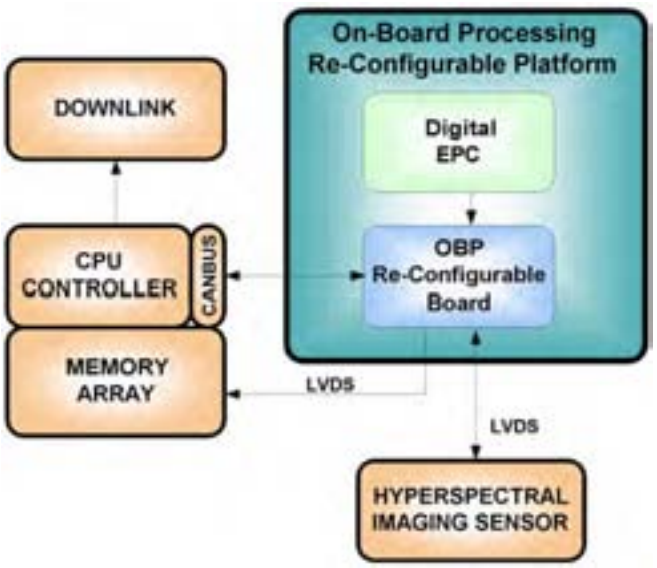

Figure 5

The future of reconfigurable platforms in space

While reconfigurable platforms offer significant advantages, the challenges mentioned herein need to be overcome before reaping the benefits. These obstacles differ from those of traditional systems but are not insurmountable, as several mitigation techniques show. With space-ready platforms that have undergone verification and testing, such as MDA's OBP Reconfigurable Platform, taking full advantage of this new technology is closer than ever.

Giovanni D'Aliesio *is a digital engineer for MacDonald, Dettwiler and Associates Corporation. He has been involved in the design and testing of space hardware, primarily for MDA's electronics contribution to the International Space Station, for the past seven years. Giovanni holds a BEng in Electrical Engineering from McGill University and an MEng in Electrical Engineering from Concordia University.*

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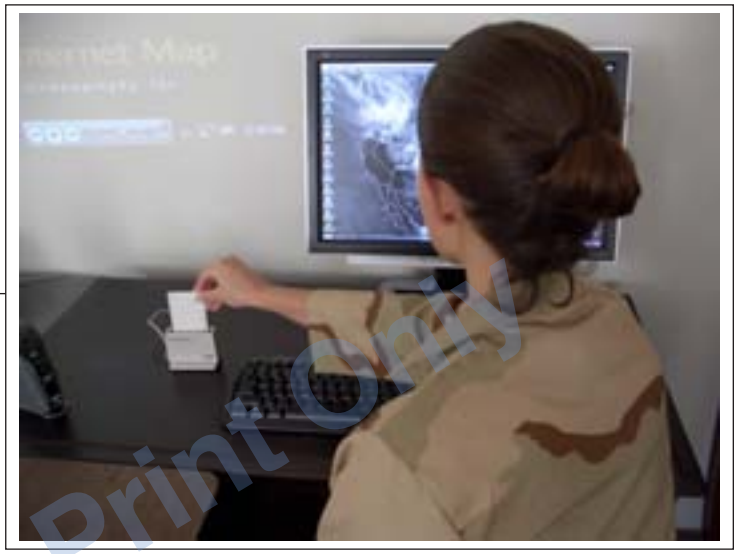
Washable smart card readers:
Cleaning up a security site and keeping it operable

By Joseph H. Carabello



Smart card technology use is increasing as a means of providing data security electronically. Washable smart card readers are of fundamental value in the military because they can be quickly cleansed from the effects of harsh environmental conditions and contamination. Several standards are in place to designate which smart card readers are most appropriate for government or military use.

Smart card technology is becoming increasingly valuable in today's military and government sectors. A *smart card* is a small, digitally encoded electronic device about the size of a credit card that contains electronic memory and possibly an embedded integrated circuit.

A smart card contains a variety of information about the individual(s) authorized to use it. For example, the information may include access codes for opening doors, account numbers, or information needed to gain access to a personal computer. Smart cards are also proving valuable in military and government applications. In fact, Homeland Security Presidential Directive HSPD-12, which sets guidelines for a federal government standard identification (ID) system, is the impetus for an ID card system for all federal employees and government contractors and is based upon smart card technology.

To use a smart card, either to pull information from it or add data to it, the user needs a *smart card reader,* a small device into which the smart card is inserted. Since smart cards and smart card readers are handled by many individuals on a daily basis, they are exposed to user-borne and environmental bacteria. They are also likely to be exposed to harsh climatic environments and biohazard threats in military and government usage.

While washable smart card readers are now available (Figure 1), the need for washable smart cards remains. It will be up to those who manufacture the cards themselves to develop a product that can be cleaned and disinfected without impacting utility. Washable readers can only address one aspect of the potential contaminants; now it is up to industry innovators to develop a comparable solution.

Figure 1

Smart cards and government security

While the President, Congress, and the public today debate the continuation of the current military position in Iraq and Afghanistan, our military men and women are still contending with the vagaries of weather and its effect on equipment – not only tanks and missiles, but computer technology such as smart cards and smart card readers.

Smart card technology, invented in the 1970s and widely used around the world, is experiencing a rebirth in the United States in the aftermath of 9/11 and subsequent security concerns.

In the United States, smart card acceptance and adoption have traditionally been slow – until now. In a scramble to comply with the Federal Information Processing Standard (FIPS) Personal Identity Verification (PIV) requirements (FIPS-201) to improve the identification and authentication of federal employees and contractors for access to federal facilities and information systems, federal agencies are seeking the most advanced smart card reader/writer technology.

Smart card implementation in Europe is far more advanced than it is in the United States. There, the technology is recognized as the standard for numerous financial and health care services. Smart cards are also used in Europe in varied common applications ranging from set-top TV boxes and vending machines to laundromats and mass transit.

Conventional smart card readers appropriate for government use should:

- Be a standard Chip/Smart Card Interface Device (CCID). This class driver reduces the need for a device-specific driver for smart card readers, lowers costs, improves driver and system stability, and leads to a simplified plug-and-play experience for users.
- Be EMV certified. Europay, MasterCard, VISA (EMV) is a standard for interoperation of "Chip or Smart cards" for authenticating credit and debit card payments. The EMV standard allows for secure interoperation between EMV-compliant cards and EMV-compliant credit card payment terminals throughout the world.

These plug-and-play readers should be designed for use with personal computers that have a USB 2.0 interface capable of reading memory and microprocessor cards. For widespread applications in military settings, these readers should also be designed to meet all major standards such as ISO 7816, EMV 2000, Microsoft WHQL, HBCI (Home Banking Computer Interface), PC-2001, IP-66, and NEMA 4X (see Table 1).

Standard	Description
ISO 7816	An international series of standards managed jointly by the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC). Defines Smart card/reader physical shape, position and shape of electrical connectors, electrical characteristics, communications protocols, command format, robustness, and functionality.
EMV 2000	Europay, MasterCard, and Visa (EMV) developed the specifications for the use of smart cards as payment cards used as either a debit or credit card. The first EMV system was released in 1994 and subsequently updated.
Microsoft WHQL	Many software products are written to work with Microsoft Windows operating systems. The majority of them are written based on Microsoft specifications but not officially tested and certified by Microsoft. Products certified by Microsoft are fully tested to work in Microsoft operating systems, significantly reducing compatibility issues.
Home Banking Computer Interface (HBCI)	An open protocol specification, publicly available and designed by two German banking companies – Sparkasse and Volksbanken und Raiffeisenbanken – and German higher-level associations such as the Bundesverband deutscher Banken e.V.
PC-2001	A set of design requirements and recommendations assembled by Microsoft and Intel and aimed at simplifying setup and use of personal computers by maximizing cooperation between the operating system and hardware.
IP66	A rating from the IEC that indicates that products are protected against the ingress of dust and high-pressure water jets from any direction.
NEMA 4X	Primarily provides a degree of protection against corrosion, wind-blown dust and rain, splashing water, hose-directed water, and damage from external ice formation.

Table 1

With current efforts focused upon an expanding array of authentication and enhanced security applications for smart card technology, industry experts – in and out of the military – are voicing concerns over the reliability and safety of smart card readers, particularly in high-traffic applications, multiple user settings, and environments with high concentrations of airborne contaminants such as dust, sand, and soot. The ability to clean and disinfect smart card readers in these venues is, therefore, mandatory.

Redesigned for today and the future

Optimally, smart card readers should complement fundamental security functionality with design features that enhance their usefulness in government/military settings – offering an additional level of product dependability as well as protection for users.

In a kerosene-heated guard tower in Korea, in the Philippines during rainy season, or out in the battlefield in Iraq – washable smart card readers deploy innovative technology to meet the stringent security demands of DoD-use settings while offering recourse for military personnel to easily cope with soot, moisture, sand, or cross-contamination challenges.

The smart card reader's washable product design seals and protects smart card reader hardware from liquid or airborne penetration; they can be disinfected or cleaned under running water. This technology reduces the likelihood of compromised use in harsh operating environments.

Military standards

Military standards/specifications for ruggedized testing of mobile computer equipment establish stringent performance and manufacturing guidelines that include a wide range of environmental factors such as contamination by fluids, rain, immersion, humidity, salt, fog, sand, and dust.

Standards are in place for evaluating technology with regard to its placement in varying altitudes and temperatures, as well as exposure to rain and dust, changes

in humidity, cold storage environments, and the impact of vibration, thermal shock, or being dropped. For example, tests are recommended in low-pressure (altitude) chambers to determine if the test item can withstand and operate in a low-pressure environment; other tests are designed to simulate land operation at high altitudes. (When used in passenger aircraft, low pressure should not be experienced.)[1]

Compliance with these test standards minimizes the danger of stubborn debris particulates destroying the functionality of data input and security devices, including smart card readers.

Smart card continues to provide security, durability

Washable smart card technology represents an effective level of security and authentication, as well as an ideal system for managing transactional data. Whether using smart card readers to initiate access authentication, network log-on, encryption, or smart card Internet transactions, federal employees, military personnel, and contractors who rely upon washable smart card readers can enjoy product functionality and durability in harsh environments while mitigating the threats of contagion.

Joseph H. Carabello, *director of Unotron, has an extensive background in computer input devices and peripherals and has been involved in health care technology business ventures. A military veteran, Joseph received training at the U.S. Army Administrative School at Fort Dix, NJ. He holds a BA in Marketing and an MBA.*

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FPGA-BASED SINGLE CHIP CRYPTOGRAPHIC SOLUTION (U)

By Mark McLean and Jason Moore

(U) ABSTRACT

(U) The use of Field Programmable Gate Arrays (FPGAs) in Type I Cryptographic equipment has historically been limited. While FPGA use is allowed, restrictions on how they are used can result in inefficient processing and an increase in system size, weight and power. For example, redundancy and isolation of functionality is required through physically separate devices. This paper introduces new technology that will provide the industry with an FPGA-based single chip cryptographic solution.

(U) The National Security Agency (NSA) and Xilinx have been working together to bring the advantages of FPGA technology to the High Assurance industry. Utilizing the Xilinx Virtex-4 FPGA, the NSA and Xilinx have developed a design flow and verification process based on NSA requirements for high-grade cryptographic processing. This paper will outline the design flow process and summarize the results of the evaluation effort.

(U) INTRODUCTION

(U) The flexibility of Programmable logic affords the Aerospace and Defense Industry many advantages. However, in certain applications like Information Assurance, government contractors and agencies have not been able to realize the full capability of programmable logic due to isolation, reliability and security concerns.

(U) In an effort to address these concerns, the NSA and Xilinx worked together to analyze and evaluate the Xilinx Virtex™-4 series of FPGAs. The goal of this analysis was to understand the design, construction, and functionality of the Virtex-4 such that a solution could be developed that would allow independent functions to operate on a single chip. Examples of such applications include, but are not limited to: Redundant Type I encryptors operating on a single chip, Red and Black data resident on a single chip and functionality operating on multiple independent levels of security on a single chip.

(U) The successful completion of the isolation analysis against the NSA Fail Safe Design Assurance (FSDA) specifications, and an exhaustive vulnerability assessment, has allowed the NSA and Xilinx to develop new technology for the industry. This paper will summarize the analysis completed and then describe, in detail, the design flow required to realize the solution.

(U) VIRTEX-4 FPGA Overview

(U) The Virtex™-4 family is Xilinx's 90nm Field Programmable Gate Array (FPGA) technology. It is based on an innovative Advanced Silicon Modular Block or ASMBL™ column-based architecture. Virtex-4 FPGAs contain three families or platforms: LX, SX and FX. The Virtex-4 LX devices are logic-centric with a high ratio of logic and I/O to feature. The Virtex-4 SX devices are signal processing-centric with a high ratio of embedded signal processing elements and internal memory to logic. The Virtex-4 FX devices are System-on-a-chip (SoC) solutions that include embedded PowerPC™ processors, Tri-Mode Ethernet MACs and 6.5Gb/s serial transceives. Virtex-4 devices are produced on a 90-nm copper process using 300mm (12 inch) wafer technology.

(U) SINGLE-CHIP ISOLATION ANALYSIS

(U) The level of logical and functional isolation that can be achieved within a single Virtex-4 FPGA was one of the critical analyses performed. The complexity, and sheer density, of the Virtex-4 device would seem to preclude any efficient isolation analysis. In addition, the difficulty in performing such an analysis is assumed to be magnified considering there are seventeen FPGAs total in the Virtex-4 family. However, Xilinx FPGAs are very modular devices. No matter which device is chosen, they consist of the same basic building blocks tiled over and over again. In the Virtex-4 FPGA, the basic building block is a Configurable Logic Block (CLB). As shown in Figure 1, the CLB includes a Global Switch Matrix (GSM) used for interconnect that is common for all features in the FPGA. In other words, the exact same GSM is used to provide interconnect from CLB to CLB, or from any CLB to dedicated functions within the FPGA like embedded PowerPC™ processors, Digital Clock Managers (DCM), DSP48 Blocks, etc. Therefore, the isolation analysis focused on an exhaustive review of the CLB and GSM.

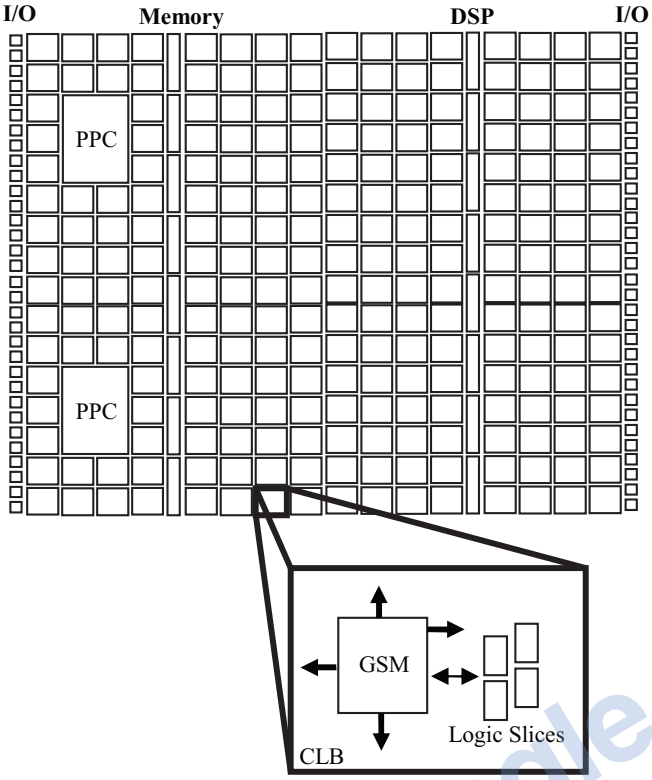

Figure 1. (U) The GSM is common to all features in the FPGA and hence was the focus of the isolation analysis.

(U) In order to achieve isolation within a single device the concept of a *fence* is introduced. The *fence* is nothing more than a set of unused CLB(s). In the *fence*, no routing or logic may be present. The result of the analysis showed that a single unused CLB between isolated regions provides, at a minimum, three physical failures of isolation, and hence exceeds the FSDA requirements. A hypothetical FPGA design with three isolated regions, separated by the fence, is shown in Figure 2.

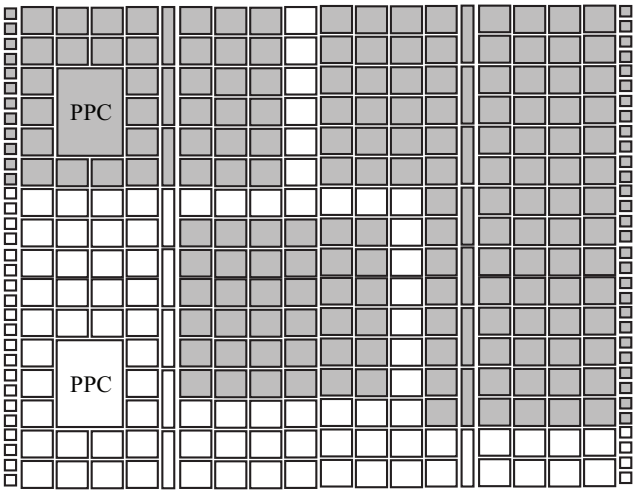

Figure 2. (U) User-defined isolated regions must be separated by one unused CLB to meet FSDA requirements.

(U) The determination of the number of unused CLBs to constitute a reliable fence meeting the FSDA requirements is but one part of the solution. This assumes that the FPGA development tools can then control the placement of logic and routing to keep the CLB completely unused. In addition to controlling the logic and routing, verification of the implementation is also required.

(U) Historically, Xilinx development tools have provided FPGA designers very granular logic placement. However, the same level of routing control has either been non-existent or left to only those with an in-depth understanding of very complicated routing constraints. Recently, Xilinx has invested in the maturation of its Partial Reconfiguration (PR) technology. This technology allows for a portion of the FPGA to be re-configured, while the rest of the FPGA operates normally. This technology is applicable to Information Assurance applications for two reasons. First, it will provide the ability to support algorithm agility – the ability of adding and tearing down multiple algorithms in a single FPGA without disrupting those that are actually processing data. Second, in order to reconfigure a portion of the FPGA, without disrupting the remaining circuits, a level of isolation must exist, and hence routing must be controlled. Therefore, by using the PR Design Flow and Toolset, both logic and routing can be controlled to create a *fence* between isolated regions in a single chip.

(U) SINGLE CHIP Design Flow

(U) Leveraging the Partial Reconfiguration capability and design tools for Virtex-4, a user can develop isolated regions of logic within a single FPGA. As mentioned earlier, the PR toolset provides the user the ability to contain routing within a specific region. In addition to the PR toolset, a couple of unique capabilities have been added.

(U) A new design constraint, called NOBOUNDARYCROSS, instructs the Place and Route (PAR) tools to keep the entirety of a route within a specified area. This is important as the tools now see the entire interconnect as a utilized route, whether it is or not. For example, a certain type of route in the FPGA, known as a HEX route shown in Figure 3, traverses from a single source to two destinations that are three and six CLBs away.

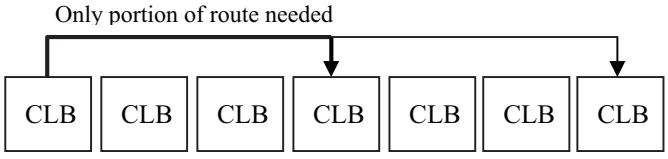

Figure 3. (U) PAR Tools understand that the entirety of a given route is used even when only a portion is needed.

(U) If a signal placed on this route gets off at the destination only three CLBs away, the router understands that the entirety of the route is actually used. Therefore the placement is constrained such that the entirety of the route is contained within the isolated

region and no part of the HEX line is allowed to cross the user-defined boundary.

(U) Another significant addition to the PR toolset was the ability to instantiate user inputs and outputs (I/O) in lower level Hardware Descriptive Language (HDL) modules. Isolated logic is defined in the PR flow through hierarchy and lower level HDL modules. For isolation to be maintained to the boundary of the FPGA, the I/Os must be contained within the isolated regions. The only way to include the I/Os in the isolated regions is to allow the user to infer I/Os in lower level HDL modules. This is done with a simple attribute statement to allow the FPGA designer the ability to create generic HDL and simulate the design as normal.

(U) Single Chip-Isolation Verification

(U) Once the design running on the FPGA has been completed it is necessary to ensure that the isolation designed into the solution still exists and has not been compromised. Xilinx's FPGAEditor tool provides a compelling visual representation of the placement and routing of the design.

(U) However, FPGAEditor presents an abstract view of the actual silicon and does not display all the information needed for isolation verification. Therefore, Xilinx has developed a verification tool for NSA known as IVT (Isolation Verification Tool) to address this issue.

(U) The IVT was developed independently from the Xilinx® ISE™ software but utilizes the same FPGA design database and code libraries. IVT can be used in two different ways. First, IVT is used to analyze the final FPGA design to ensure the isolation designed into the FPGA, did not get comprised due to errors in the design flow. Second, IVT can be used early in the design process to identify potential mistakes before releasing a Printed Wiring Board (PWB) to fabrication and working through the FPGA implementation process.

(U) When analyzing the final design, the placed and routed designs from the Partial Reconfiguration Design Flow are inputs into the IVT. In this design flow, a design database, also known as an .ncd file, will exist for each isolated region, and the complete merged design. Knowing what functionality exists in each isolated region, and how the isolated regions have been merged to form one final design provides all the information that is required by the IVT to verify isolation. IVT performs an exhaustive analysis tracing every potential interconnect path that could be created to determine if the hypothetical interconnect would cause the isolation to be compromised. If a path between regions could exist within less than a user defined number of failures, IVT will generate an error and report the hypothetical failing path to the designer.

(U) In addition to the logic and routing isolation analysis, the IVT also analyzes device pin and package locations to ensure that if red and black data exist in the same FPGA, red I/Os and black I/Os do not share the same bank and are not physically adjacent in both the silicon and at the device package (i.e. the ball of the FPGA Ball Grid Array (BGA) package).

(U) As mentioned earlier, the IVT can also be used to identify potential problems early in the design flow process. IVT can analyze an FPGA Designers User Constraint File (.ucf). The constraints file is how the system designers creates isolated regions in the FPGA with proper logic and routing placement. The analysis can be done early in the design process, which will help eliminate costly PWB layout mistakes.

(U) Communication between isolated regions

(U) Communication between isolated regions is expected for applications such as the transfer of keying material or the comparison of redundant encryptors output. In these scenarios the use of Bus Macros are required.

(U) Bus Macros, as shown in Figure 4, are small pieces of IP that are pre-designed by Xilinx, analyzed by NSA, and then used by the FPGA designer. Since they are designed in advance and provided in the form of an .nmc file, they are considered hard macros since the logic and routing used is pre-defined. The value of the Bus Macro is that it eliminates un-deterministic routing behavior when providing a communication path between isolated regions. Bus Macros are commonly used in commercial Partial Reconfiguration applications. A set of special Bus Macros have been designed by Xilinx to meet the FSDA requirements.

(U) There are a number of different bus macro types varying in direction, data width, asynchronous vs synchronous and with and without enables.

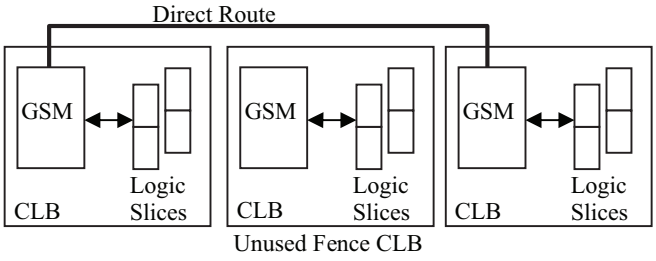

Figure 4. (U) Logical representation of a Bus Macro

(U) SECURITY EVALUATION

(U) Before a device can be used in a U.S. cryptosystem, a thorough security analysis must be completed. This analysis is conducted to determine the level-of-effort required by an adversary to exploit the device. As a result of the analysis, strategies can be developed and deployed to strengthen system security. FPGA technology is critical to future crypto system development and the Xilinx Virtex-4 (V4) was the most comprehensive FPGA evaluation done to date. The evaluation results and test setups are available from NSA with the proper clearance and a valid need-to-know.

(U) The Virtex-4 was tested against publicly known vulnerabilities such as Differential Powerline Analysis, Transient Fault Analysis and JTAG attacks. The device was also tested to ascertain remenance issues within the V4's SRAM cells that could potentially be exploited by an adversary. The remenance evaluation is focusing mainly on the Battery Backed RAM (BBR), and will include a cursory evaluation of the configuration RAM. Additionally, NSA applied classified in-house developed evaluation techniques in an attempt to better quantify the overall security of the V4.

(U) The evaluation also included analysis of the Verilog code used to synthesize the V4's control, security and AES key programming functions. These functions are critical to the secure operation of the device.

(U) Due to the high security requirements of U.S. crypto equipment, a security monitor was developed to be implemented within the V4 fabric to further enhance security. The monitor will always be vigilant and handle all security related functions for the device. This IP core will remove the burden of physical security requirements from the system designers and allow them to concentrate more on their particular application. The security monitor will be embedded into all designs processing sensitive data. The security monitor will be ITAR controlled and will be available from Xilinx.

(U) When used in conjunction with the security monitor, NSA found the V4 to be a robust architecture capable of processing classified information and maintaining a very high level of security.

(U) SUMMARY

(U) Working together, NSA and Xilinx have developed technology that will enable the Information Assurance industry to maximize the advantages of programmable logic. Using published design guidelines, verification tools and the Security Monitor IP, Xilinx Virtex-4 FPGAs can be used to support redundancy, red/black data, and multiple levels of security on a single chip.

Mark McLean *is a technical director for the National Security Agency. He is responsible for microelectronic evaluations of devices that are used in secure systems, and his guidance not only supports the Information Assurance Directorate at NSA, but the entire U.S. government and its NATO allies. He has more than 10 years of experience in his present field and more than 23 years of experience as a design engineer. He has a Bachelor's in Computer Science from National University, a Master's in Computer Engineering from Loyola, and is currently working on his PhD in Computer Science, focusing on neural networks, at the University of Maryland at College Park.*

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Jason Moore *is a program manager in the Aerospace and Defense Division of Xilinx, responsible for FPGA technology development in support of major DoD Transformation programs (primarily the Joint Tactical Radio System and crypto modernization). Previous to Xilinx, Jason was responsible for the development of FPGA-based communication security equipment in a wide range of avionics and ground-based platforms at the Motorola Government Group. He was awarded two U.S. patents on cryptographic design and has a patent application pending for novel approaches to address logical and functional isolation within a single FPGA. Jason has 14 years of experience in the aerospace and defense field and holds a BSEE from New Mexico State University.*

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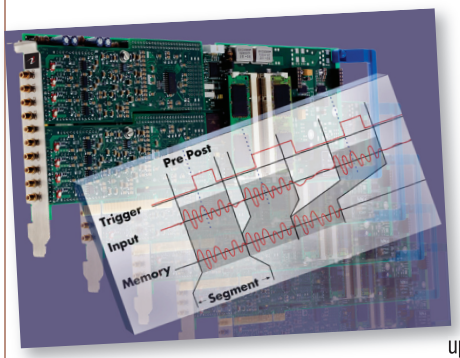
Editor's Choice Products

By Sharon Schnakenburg

Multiple Recording option stops the do-overs



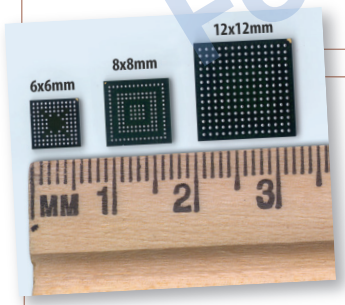
A songwriter once penned, "starting over is hard to do" (or was that "breaking up is hard to do?"). And watching the TV reality series by the same name, "Starting Over," is an even more arduous task...

Well now vendor Strategic Test is on the same wavelength as the aforementioned: Their new Multiple Recording option for the UF2 series of PCI-based, 66 MHz oscilloscope/digitizer cards is designed to eliminate annoying hardware restarts between waveforms in radar applications. [Though its 16 MHz Pulse Repetition Frequency (PRF) also makes it a viable contestant in sonar, lasers, ultrasound applications, and ordnance detonation events.] The firmware-implemented Multiple Recording option enables cards to re-arm in time for the next event within only four clock cycles, so that no events are missed. External triggering ability and multiple triggers also add flexibility to synch test equipment with other equipment and capture events dictated by other systems.

The Multiple Recording option is available for all Strategic Test's UltraFast 8-, 12-, 14-, and 16-bit resolution oscilloscope PCI cards but varies by model. The option can be purchased with the card initially or added later.

Strategic Test
www.strategic-test.com
RSC# 32890

Don't "super size" it – we'll take a small



In the world of fast food restaurants, "super size" seems to be the order of the day. But in the world of FPGAs, does the same logic apply? Not necessarily. Take, for example, QuickLogic's new 6 x 6 mm and 8 x 8 mm small form factor versions of their PolarPro and Eclipse II FPGAs. Although larger form factor FPGAs by Altera and Xilinx are market "heavyweights," QuickLogic's smaller form factor FPGAs have the advantage of fitting well into space- and power-constrained applications: PMC modules, interface boards, or inside remote sensors. They are also extremely useful for control signal handshakes and interface "mating."

Other charms of QuickLogic's smaller FPGAs include the Eclipse II's low standby currents of 14 µA, while the PolarPro's Very Low Power (VLP) mode enables a low draw of 2.2 µA, saving battery power. Both devices are also supported by QuickWorks 9.8.2 and System General tools.

The Eclipse II QL8150 and PolarPro models QL1P075, QL1P100, QL1P200, and QL1P300 are available at 8 x 8 mm, and the Eclipse II QL8050 comes in a 6 x 6 mm form factor.

QuickLogic Corporation
www.quicklogic.com
RSC# 32893

Is less really more?

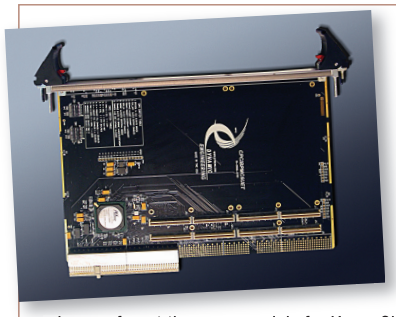
For years, minimalists have touted the old adage "less is more." Now it looks like SiliconSystems just may be proving them right: The company recently released a 1.8" form factor version of their SiliconDrive storage device, which will boldly go where no 2.5" form factor has gone before.

Ideal for space- and weight-constrained spaces including in-flight applications, notebook and tablet PCs, and portable medical devices, the 1.8" SiliconDrive provides cutting edge solid-state storage. Of course, that is synonymous with higher levels of reliability and robustness in rugged military applications. And this device is no dummy. It stores a whole 16 GB of storage, as compared to typical rotating media hard drives that provide about 8 GB.

Other pluses of the 1.8" SiliconDrive include SiliconSystems' PowerArmor and SiSMART technologies, which are designed to eliminate the field failures that can result from power disturbances, provide increased security for software IP and application data, and eliminate the need for product requalifications. So do *less* size and weight really provide *more* benefits? In this case, we'd have to say yes.

SiliconSystems
www.siliconsystems.com
RSC# 32892

"Glue" carrier joins CompactPCI boards and PMCs



We all remember Elmer's glue from grade school days. And who can forget the commercials for Krazy Glue featuring a man suspended in mid-air by his forearms from the surface above him?

While Dynamic Engineering isn't claiming its new product can suspend a man's entire body weight mid-air, they *are* claiming that their new cCIBPMC6U-ET 6U bridged dual PMC carrier can act as a "glue" or bridge between extended temperature CompactPCI boards and PMCs.

While PMC carriers are not the most "eye-catching" product, they are, of course, an absolute necessity for PMC interfacing. Since this carrier features a rugged CompactPCI form factor, the proverbial door is opened even wider to military communications systems designers, giving them the affordability advantage of using CompactPCI COTS boards. The cCIBPMC6U-ET also provides more design choices to users through its differing bus speeds, maximizing the number of PMCs that can be used. (The CompactPCI and PMC buses can both run at 66 or 33 MHz.)

Other honorable mentions include an operating temperature range of -40 ˚C to +85 ˚C, signal conditioning, DMA support, and a low-power design: +5, +3.3, +12, -12V, and user-selectable VIO of 3.3 or 5V to the PMC.

Dynamic Engineering
www.dyneng.com
RSC# 32891

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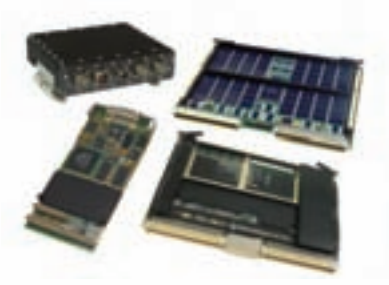


RSC# 45 @ www.mil-embedded.com/rsc

Military and avionics interfaces

Form factor	Company/ Web address	Model	Description	MIL-STD-1553 interfaces	ARINC-429 interfaces	AFDX interfaces	Ethernet ports	Serial ports
Chassis/ System	Mobility Electronics www.magma.com	Magma PCI Expansion Chassis	PCI Expansion Chassis series that enables designers to add legacy PCI cards to PCIe computers	•	•			
CompactPCI	AcQ InduCom www.acq.nl	CPCI1403 MIL-STD	An intelligent interface card providing full MIL-STD-1553 test, simulation, and bus analysis capability for the CompactPCI bus, with 1553A, 1553B, McAir, and STANAG 3838 capability on a single card	•				
CompactPCI	AcQ InduCom www.acq.nl	CPCI2403 MIL-STD	An intelligent interface card for two serial, dual redundant MIL-STD-1553 data buses and the CompactPCI bus	•				•
CompactPCI	AcQ InduCom www.acq.nl	CPCI302 ARINC-429	An ARINC-429 controller for CompactPCI		•			
PC/104	BMC Communications www.bmccorp.com	UADI 1553 ARINC RS	A PC/104 Universal Avionics Digital Interface (UADI)	•				
PC/104-*Plus*, PCI-104	Condor Engineering www.condoreng.com	CEI-430	High-density, intelligent ARINC-429 interface for PC/104-*Plus* or PCI-104		•			
PCI	AcQ InduCom www.acq.nl	PCI1403 MIL-STD-15	An intelligent interface card providing full MIL-STD-1553 test, simulation, and bus analysis capability for the PCI bus standard, with 1553A, 1553B, McAir, and STANAG 3838 variants in one card	•				
PCI	AcQ InduCom www.acq.nl	PCI2403 MIL-STD-155	An intelligent interface card for two serial, dual redundant MIL-STD-1553 data buses and the PCI bus	•				•
PCI	AcQ InduCom www.acq.nl	PCI302 ARINC-429	An ARINC-429 controller for PCI		•			
PCI	AIM-USA www.aim-online.com	API-FDX-2	A two-port AFDX test and simulation module for the PCI bus			•		
PCI	Alphi Technology www.alphitech.com	PCI-1553-PLX-x	MIL-1553 with UTMC BCRTM controller	•				
PCI, 3U and 6U CompactPCI, 3U and 6U VME	AcQ InduCom www.acq.nl	M302 ARINC-429	An ARINC-429 Controller M-module based upon the Motorola MC68332 microcontroller		•			
PCI-X	AIM-USA www.aim-online.com	APX1553	PCI-X compatible cards for MIL-STD-1553 test, simulation, and monitoring applications	•				
PMC	AcQ InduCom www.acq.nl	PMC403 MIL-STD-1553	An intelligent interface card providing full MIL-STD-1553 test, simulation, and bus analysis capability for the PCI mezzanine standard, with 1553A, 1553B, McAir, and STANAG 3838 variants in one card	•				
PMC	Condor Engineering www.condoreng.com	CEI-830	An ARINC high-density interface for PMC		•			
PMC	GE Fanuc Automation www.gefanuc.com/ embedded	EPMC-1553	An eight-channel, high-density PMC card for MIL-STD-1553B Notice II	•				
Proprietary	AcQ InduCom www.acq.nl	M303 MIL-STD-1553	An intelligent interface card providing full MIL-STD-1553 test, simulation, and bus analysis capability for the M-module standard, with 1553A, 1553B, McAir, and STANAG 3838 variants in one card	•				

Form factor	Company/ Web address	Model	Description	MIL-STD-1553 interfaces	ARINC-429 interfaces	AFDX interfaces	Ethernet ports	Serial ports
Proprietary	AcQ InduCom www.acq.nl	USB403	A portable interface unit providing full MIL-STD-1553 test, simulation, and bus analysis capability in a compact, self-contained unit, to connect via a USB interface to suitable host systems	•				
Proprietary	Condor Engineering www.condoreng.com	FlightCORE-1553	Intellectual Property (IP) that implements MIL-STD-1553 core functions for use in Altera and Xilinx FPGAs	•				
Proprietary	Radstone Embedded Computing www.radstone.com	AFIXM	An addition to the AFIX (Additional Flexible Interface Xtension) family of plug-on daughtercards	•				
System	CES www.ces.ch	CES Mission Computer Family	Ready-to-go platforms for rugged computer systems	•	•	•		
VME	AcQ InduCom www.acq.nl	VME2303 MIL-STD	An intelligent interface card for two-channel, dual redundant MIL-STD-1553 applications	•				
VME	AcQ InduCom www.acq.nl	VME302 ARINC-429	A 6U or 3U VMEbus board		•			
VME	Aitech Defense Systems www.rugged.com	C437	A rugged, low power 6U VMEbus board that provides multiple I/O capabilities, including ARINC-429, analog-to-digital, digital-to-analog, audio, and discretes		•			
VME	Ballard Technology www.ballardtech.com	OmniBus VME	A family of avionics databus interfaces for MIL-STD-1553, ARINC 429, and other aircraft I/O interfaces	•	•		•	•
VME	GE Fanuc Embedded Systems www.gefanucembedded.com	AFDX-E1000	An intelligent and flexible AFDX end system with a single or dual channel	•		•	•	
VME	ITCN www.itcninc.com	SystemTrace 1553	A module capable of monitoring and recording activity on up to eight dual redundant MIL-STD-1553 buses		•		•	
VME/VXI	Data Device www.ddc-web.com	BU65527/28	Intelligent interface between multiple, dual-redundant MIL-STD-1553A/B Notice 2 data buses and parallel VMEbus and VXIbus		•			
VME/VXI	Data Device www.ddc-web.com	BU-65570V-72V	VME/VXI card designed for test and simulation of MIL-STD-1553 systems	•				
VME/VXI	Data Device www.ddc-web.com	BUS 65536	C-size, 16-bit VXIbus printed circuit card for testing and simulation of MIL-STD-1553 systems	•				
VXI	DIT-MCO International www.ditmco.com	R-2175	The rugged, military version of a portable unit that tests relay panels, control panels, junction boxes, electrical chassis, and other electrical and electronic subsystems	•				
VXI	Excalibur Systems www.mil-1553.com	EXC 3000VXI	Multiprotocol interface for VXI	•	•			
VXI	Interface Technology www.interfacetech.com	IBE4080 Xtreme Bus Emulators	Bus emulators that are software programmable for arbitrary bus emulation	•				•
VXI	Western Avionics www.western-av.com	IIB-1553-VXI 4C	An intelligent interface card that provides four independent channels for full MIL-STD-1553 test, simulation, and bus analysis functions on the VXIbus	•				

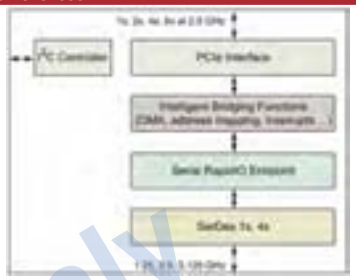
Data was extracted from OSP's product database on Feb. 21, 2007. Description keywords searched include MIL-STD-1553, AFDX, avionics, and ARINC products entered 1/1/06 through search date within *VME and Critical Systems, Military Embedded Systems, CompactPCI and AdvancedTCA Systems,* and *PC/104 and Small Form Factors* magazines. Entries were further edited for relevance to product guide's theme. OpenSystems Publishing is not responsible for errors or omissions, and vendors are encouraged to add their new products to our website at www.opensystems-publishing.com/vendors/submissions/np/.

New Products

By Sharon Schnakenburg

BRIDGE: SERIAL RapidIO-TO-PCI EXPRESS CORE

Mercury Computer Systems, Inc.
Website: www.mc.com
Model: Serial RapidIO-to-PCIe Intelligent Bridge Core
RSC No: 32609



A Serial RapidIO-to-PCIe intelligent bridge core • Available as Verilog HDL in either Synopsis or Synplicity synthesis environments • Core can be implemented in FPGAs, ASICs, ASSPs, or SoC devices • Multiple DMA engines, Serial RapidIO mailboxes and interrupts, address mapping, and sophisticated queuing within the intelligent bridge assure high utilization while maintaining maximum port bandwidth • Core connects a Serial RapidIO port (RapidIO 1.2) operating at up to 3.125 GHz to an x8 PCI Express port (PCI Express 1.1) operating at 2.5 GHz through a nontransparent bridge • Verilog HDL targets FPGAs from Altera, Lattice, and Xilinx, and 0.09 micron (or smaller) line width geometries for custom silicon implementations

CARRIER BOARD: AdvancedMC

VadaTech Inc.
Website: www.vadatech.com
Model: AMC090 **RSC No: 32388**

Optically isolated digital input AdvancedMC module • 16-channel optically isolated digital inputs • Eight TTL/CMOS channels • Eight 0 V to 10 V channels • Software-programmable functions include programmable debounce, programmable COS interrupts (rising edge, falling edge, or level sensitive), and multichannel input masked interrupts • I/O connectivity is via a high-density rugged front-panel connector • Utilizing VadaTech's patent pending board design, the AMC090 is available in a single-width half-height AdvancedMC form factor, which allows for higher-density I/O applications • AMC.0 compliant • IPMI 2.0 compliant • RoHs compliant • Conformal coated option

ENCLOSURE

Mobility Electronics, Inc.
Website: www.magma.com
Model: Magma PCI Expansion Chassis RSC No: 32610

PCI expansion chassis series that enables designers to add legacy PCI cards to PCIe computers • Just about any type of PCI card can be used – ranging from audio, video, graphics, test and measurement, data acquisition, SCSI, Fibre Channel, SATA, and military interfaces such as ARINC 429 and MIL-STD-1553 • Chassis' x1 PCIe connection is compatible with any single PCI Express slot, and the chassis is easily recognized by the host computer via plug-and-play installation • PCI backplane supports 5 V, universal, and 3.3 V PCI and PCI-X cards • Available in 4U and 2U rack-mount configurations • Backplanes available in configurations of 4, 6, 7, and 13 slots

Triple E
Website: www.tripleEase.com
Model: 1U Microchassis RSC No: 32402

1U microchassis suitable for rugged applications • Addresses inherent problems associated with electronic systems configured for military, aerospace, commercial, and industrial harsh environment applications • Meets IEEE1101.10 and IEEE1101.11 mechanical requirements • Configured with VME64x, CompactPCI, or PICMG 2.16 backplane, the unit allows for up to two 6U x 1.6 mm x 160 mm size boards in front, and two 6U x 1.6 mm x 80 mm direct plug-in rear transition boards • 10.75 lbs • 19" rack-mount (L-R) x 1.73" high x 11.25" deep • 0.036" thick zinc plated steel for structural integrity • Durable powder coat finish • Removable side walls • A 3U, 300 W PICMG 2.11 compliant power supply fits compactly within the 1U rack aperture • The power supply has nominal input of 115-240 Vac, operational input of 90-264 Vac, output of +5 V/30 A, +3.3 V/40 A and +12 V/1 A with operating temperature range between -5 °C to +55 °C • Eight 12 Vdc 11.00 CFM fans via push-pull method provide reliable and efficient cooling • The unit complies with UL, EN, and CE safety specifications, and conducted and radiated EN Class B and EN ratings

EXTENDER BOARD: AdvancedMC

N.A.T. GmbH
Website: www.nateurope.com
Model: NAMC-EXT RSC No: 32812

An extender board for AdvancedMC • Provides a versatile means to speed up the development process and to troubleshoot AdvancedMC within an ATC • Support for all fabric interfaces • Management and payload power can be disconnected individually to enable power measurement • Three clock lines

GSM/GPRS MODULE

iWOW Connections
Website: www.iwow.com.sg
Model: iWOW TR-800 RSC No: 32672

A GSM/GPRS module designed to deliver high performance/upgradeability • Robust platform for easy development of machine-to-machine applications • Quad-band for wide coverage and global access • Extremely slim, measuring 3 mm in thickness • Weighs 8.3 g • Easily integrated into any environment • Two options for mounting the GSM antenna: can be mounted via onboard microminiature connector or directly on the antenna soldering pad • Enhanced reliability – Equipped with industry standard communication protocols such as TCP/IP, MMS, and Push-to-Talk, which can be embedded to simplify the data transfer process

MASS STORAGE: PLUG-IN UNIT

PQI Europe
Website: www.pqieurope.com
Model: U510 CardDrive 32GB **RSC No: 32683**

A portable storage device with a 32 GB capacity • Measures only 3 mm thin • Mobile USB flash drive, USB 1.1/2.0 compatible • Hot swappable, USB plug-and-play compatible • LED access indicator with three modes: busy, waiting, and off • Built-in personal customizable software (USB Notebook Professional)

MEZZANINE: AdvancedTCA CARD CARRIER

Extreme Engineering Solutions
Website: www.xes-inc.com
Model: XCalibur1210 **RSC No: 32821**

A versatile AdvancedTCA mezzanine card carrier • Can be factory configured to support any combination of PrPMC, XMC, and AdvancedMC modules • Four configurable AdvancedMC/XMC/PrPMC sites • AdvancedMC.1, AdvancedMC.2, and AdvancedMC.3 support • VITA 42.3 XMC support • AdvancedTCA base and fabric Ethernet support • Dual MPC7448 PowerPC processors • Full IPMI and hot-swap support • Green Hills INTEGRITY BSP • QNX Neutrino 6.3.0 BSP • Linux 2.4 and 2.6 with SMP support • VxWorks 5.5 and 6.2 with VxMP support

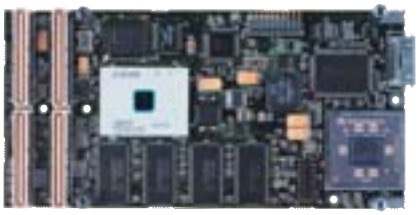
MEZZANINE: PMC

Critical I/O
Website: www.criticalio.com
Model: XGE4032 PMC **RSC No: 32801**

1 Gbps Ethernet PMC based on Silicon Stack technology • Offers fully offloaded IPv6 capability, wire-speed throughput, ultra-low host processor overhead, and low latency • Enables Ethernet data networks to satisfy even the most demanding real-time system applications such as radar, data acquisition, mission computers, sonar, FLIR, and SIGINT data, video distribution, and signal processing • Wire-speed throughput of 442 MBps • Dual-channel design • Integrated firmware-based protocol engine allows easy protocol extensions and customization • Full interoperability and compatibility with standard Ethernet components • Extensive software library and driver support for real-time and standard OS platforms

MEZZANINE: PrPMC

Motorola Inc., Embedded Communications Computing
Website: www.motorola.com/computing
Model: PrPMC8005E Processor PMC **RSC No: 32588**



High-performance Processor PMC • MPC7410 or MPC750 PowerPC microprocessor • AltiVec technology • High-performance PowerPlus III architecture • 2 MB/1 MB of L2 cache • Up to 512 MB onboard ECC SDRAM; 32 MB onboard flash; 72-bit ECC memory controller ASIC • Single-wide PMC with 66/33 MHz PCI interface • Optional 10/100BASE-T Ethernet interface • 64-bit PCI host bridge • One asynch serial debug port • Four 32-bit timers, two watchdog timers

MICROCONTROLLERS

Microchip Technology, Inc.
Website: www.microchip.com
Model: PIC16F882 MCU **RSC No: 32823**

A member of Microchip's 28- and 40/44-pin PIC18F88X family of microcontrollers, for use in a wide range of applications • Provides design engineers the option to migrate to a lower-cost family member as their code development stabilizes • In turn, all five members of the PIC16F88X family maintain compatibility with other 28/40-pin PIC microcontrollers for easy migration, while providing a host of new features • Enhancements include dual internal oscillators with clock switching and fail-safe clock mode; up to 14 ADC channels; an advanced comparator module featuring two comparators and a set/reset latch to allow emulation of many analog circuits; and low-power enhancements that extend battery life • The PIC16F88X family provides a consistent peripheral set and multiple memory-size options and is complemented by a vast portfolio of pin- and code-compatible PIC microcontrollers that enable customers to quickly move to the right part for their chosen application, without having to write all new code

MULTI-ETHERNET 5.25" EmBOARD

Liantec Systems Corporation
Website: www.liantec.com
Model: EMB-5740 **RSC No: 32681**

5.25" drive-size VIA C7-Eden multi-Ethernet EmBoard with embedded Tiny-Bus modular expansion solution • 5.25" drive-size EmBoard • VIA C7-Eden embedded x86 computing platform • Onboard VIA C7-Eden CPU and 512 MB DDR2 SDRAM • Onboard four GbE interfaces • Onboard CompactFlash, SATA, and GPIO ports

(continued on page 52)

For more information, enter the product's RSC# at www.mil-embedded.com/rsc

PCI CARD

North Atlantic Industries
Website: www.naii.com
Model: 76C2 **RSC No: 32539**

Half-slot, multifunction PCI card • A/D, D/A, S/D, function generator, discrete I/O, TTL I/O, transceiver I/O, LVDT/RVDT, and RTD functions available • Interchangeable multifunction design provides extensive diagnostics • Each function is highly programmable at the channel level • Continuous background (BIT) testing performed on all functions and channels • Testing is totally transparent to the user, requires no programming, and doesn't interfere with the normal operation of the card • Suited for military and commercial programs, including airborne, shipboard, ground mobile, and C3I applications • Interchangeable modules increase functional density and reduce power consumption, size, and cost of the overall system • Available with operating temperature ranges of -40 °C to +85 °C and 0 °C to +70 °C

PROCESSORS: OPTERON

WIN Enterprises Inc.
Website: www.win-ent.com
Model: MB-06058 **RSC No: 32806**

PICMG 1.3 SBC with AMD second-generation Opteron processor • High-performance with up to 2.6 GHz processing speed • Configure with a single dual-core CPU or use optional daughtercard to support another dual-core second-generation AMD Opteron processor • Offers reduced power consumption (within a 95 W envelope) and low heat production • PICMG 1.3 form factor: 13.330" x 4.976"; 33.86 cm x 12.64 cm • NVIDIA nForce Professional 2200 chipset • Two memory slots providing up to 8 GB; optional four slots/16 GB

RUGGED COMPUTERS

Datametrics
Website: www.datametrics.com
Model: Model 9100 - EC **RSC No: 32689**

General purpose, compact, rugged embedded computer with a small footprint • Suitable for low-power, ultra-performance, space-challenged applications • Powerful Intel Pentium M 1.8 GHz and Intel Core Duo 1.66 GHz processors • 1 GB DDR SDRAM • 60 GB 2.5" HD IDE • Weighs 3.5 lbs • Wireless Internet capabilities • Designed to meet DO-160E EMI/EMC • Up to 11 various I/O ports • Compatible with a variety of operating systems

Panasonic Computer Solutions Company
Website: www.panasonic.com
Model: CF-19 **RSC No: 32840**

A rugged convertible tablet PC • Intel Core Duo processor U2400 (2 MB L2 cache), processor speed 1.06 GHz, 533 MHz FSB • 80 GB HDD • 512 MB SDRAM standard, expandable to 4,096 MB • Optional external USB combo drive • Full magnesium alloy

case with handle • 10.4" 1,024 x 768 (XGA) transmissive, daylight-readable TFT Active Matrix Color LCD with digitizer • 550 Nit LCD brightness (470 Nit with touch screen) with new low-reflection screen coating • Dimensions: 1.9" (H) x 10.7" (W) x 8.5" (D) • Weight: 5 lbs • Battery life: 7 hours, depending on use conditions • Intel PRO/Wireless 3945ABG LAN Connection 802.11a/b/g, Bluetooth v2.0 • Optional integrated WWAN (EV-DO, HSDPA) • Optional integrated GPS receiver • Security features include: 32-character password security: supervisor, user; cable lock slot; Trusted Platform Module (TPM) v.1.2 security chip, optional fingerprint scanner • Microsoft Windows XP Tablet PC Edition 2005, Display Rotation Tool

SOFTWARE-DEFINED RADIO

Pentek, Inc.
Website: www.pentek.com
Model: 7642 **RSC No: 32562**

Multichannel transceiver PCI board with FPGA • Four 125 MHz 14-bit A/Ds • Optional factory-installed IP core DDC • One digital upconverter with 500 MHz 16-bit D/A • 768 MB of DDR SDRAM • Dual timing buses for independent input and output clock rates • LVDS clock/sync bus for multiple board synchronization • 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on 64-pin DIN connector

SYSTEM MANAGEMENT

Interface Concept
Website: www.interfaceconcept.com
Model: ComEth3300b **RSC No: 32403**

A 6U/VME Fast and Giga managed Ethernet switch • Particularly suited for air- and conduction-cooled applications • High-speed, nonblocking Layer 2+ switch • 24 Fast Ethernet and 6 GbE channels • Auto-negotiation and auto-crossover for true plug-and-play • Supports VLANs based on ports or/and MAC addresses to simplify network management • Multicast's flow management with IGMP snooping, IGMP V2 • Standard, extended, and conduction-cooled grades

SYSTEMS: INDUSTRIAL RUGGEDIZED

Advantech eAutomation Group
Website: www.eAutomationPro.com
Model: UNO-3074 **RSC No: 32802**

High-performance Pentium M/Celeron M grade embedded automation computer • Two RS-232 ports, two RS-232/422/485 ports with RS-485 automatic flow control, two 10/100 Ethernet ports, four USB ports, and four PCI bus expansion slots for versatile applications • Supports Windows XP (SP2) Embedded with write protection (EWF) with a preconfigured image that has optimized onboard device drivers • Supports Windows 2000/XP and Linux • 512 KB battery-backup SRAM; anti-shock up to 50 *g* and anti-vibration up to 2 *g* • Four-channel isolated digital input, four-channel isolated digital output with timer, counter, and interrupt handling and dual power input • Open platform

Crosshairs Editorial

By Chris A. Ciufo

Ops briefing:

FCS and VPX … free software … AFCEA and AUSA … USS Ranger Museum … magazine acquisitions

There's so much going on in our embedded military industry that this month's column is intended to be something like a printed RSS feed. For our *actual* RSS feeds, check out the newswire at www.mil-embedded.com or the blog at www.VMEnow.com.

In a rare public disclosure, **Boeing** announced that the COTS standard **VITA 46 is being used on Future Combat Systems (FCS)**. Long an active participant in the VSO (www.vita.com), Boeing's all in favor of two-level maintenance, and the company recently spearheaded the VITA 48 REDI working group. Where VITA 46 – also called *VPX* – adds **hundreds of I/O pins and multiple switched serial fabrics** to a new type of VME backplane, REDI adds covers to VPX boards to provide stiffening and ESD protection for 3U and 6U LRUs. Boeing forecasts a "$4B operation and support (O&S) cost reduction for [the] Integrated Computer System (ICS) alone" in the Army's FCS program (see Figure). With **two-level maintenance**, LRUs can be swapped in the field by technicians, thus eliminating the military's middleman depot structure.

Mirroring the trend in desktop software for OS X, Windows, and Linux, COTS software vendors are starting to provide free, fully functioning versions of their embedded applications and tools. "Best software practice" vendor **Telelogic** – maker of the popular DOORS, Rhapsody, and Tau products – is offering **Telelogic Modeler for free** (www.telelogic.com). Users can use OMG's UML 2.1 to document and specify designs. Similarly, designers can download **OpenMake's** (formerly known as Catalyst Systems) **Mojo 7.0 build-to-release** automation software (www.openmakesoftware.com) for free. Mojo automates the software build process and competes with alternatives **BuildForge** and **Anthill Pro**.

I attended the recent **AFCEA West** show in San Diego and was extremely pleased to note more than 400 government and defense suppliers exhibiting and more than 10,000 attendees. In fact, parking was a challenge and traffic was jammed leading into the convention center. Naysayers argue that tradeshows are dead. Don't believe them. While there were fewer primes and PEOs exhibiting than I remember, the Boeing, General Dynamics, and

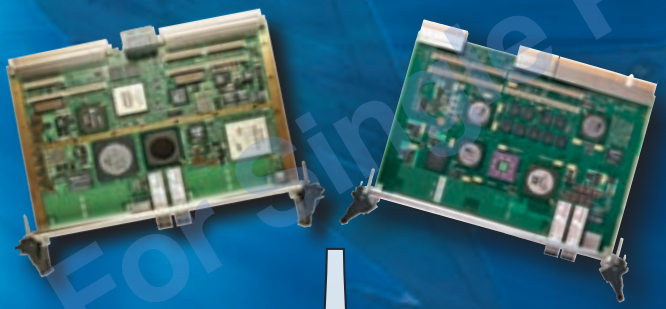
Rugged High-Speed Data Recording and Storage

10GbEthernet

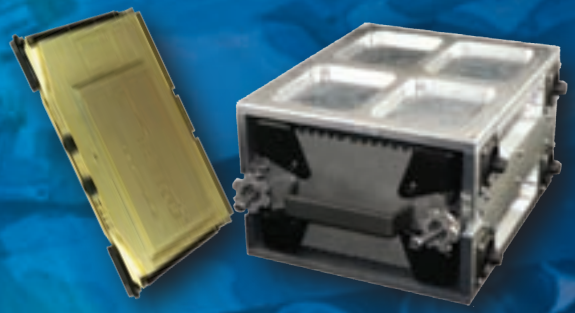
SerialFPDP

Custom

Vortex Data Recording and Playback Systems



Fibre Channel Storage Area Network



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VMETRO

innovation deployed

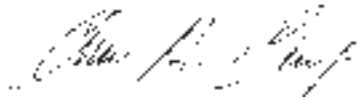
Lockheed Martin booths were awesome. In a luncheon address, representatives discussed the "1,000-ship Navy," an idea first proposed by admirals John Morgan and Charles Martoglio in 2005 (according to *Jane's Fighting Ships*). This collective of U.S. Navy, allies, law enforcement, and civilian vessels would band together loosely to police and provide homeland security on the seas and in our ports. The "1,000-ship Navy" is certainly one way to offset defense costs.

Though there seemed to be **fewer foreign uniforms attending,** there was a notable trend toward prepackaged, rugged COTS chassis. (I counted about 20 companies displaying them.) I'm also attending the **AUSA Fort Lauderdale** show in March and will report back on what's new in **Army vetronics and aviation**. Last time I attended a couple of years ago, the Army brass killed the Commanche helicopter program (in real time and right in front of our eyes!), citing recapitalization costs incurred by then-Operation Iraqi Freedom. Wonder what bombshells they have in store this year?

In other news, I've been asked to join the **USS Ranger (CV-61) Museum Foundation** (www.ussrangercv61.org), a group of local Pacific Northwest military and business professionals who are trying to bring this super aircraft carrier to the **Vancouver, Washington** area. A Forrestal-class ship, Ranger was featured in the **movie "Top Gun"** and was decommissioned in 1993. With a crew of nearly 5,000 and displacing 82,000 tons with up to 80 aircraft, the Ranger was launched in 1954 and saw action in all major theaters including Desert Storm in 1990. My involvement as a volunteer docent might be to educate the public on current military technologies and capabilities. Sounds like a lot of fun, if the foundation can raise the millions needed to bring her down from Bremerton, Washington and maintain her.

And lastly, I'm pleased to announce that *Military Embedded Systems (MES)* magazine has been growing by leaps and bounds in the past 12 months. We've "organically grown" our circulation by 20 percent as readers have voluntarily signed up to receive the magazine. Most recently, **we have acquired the assets of *MIL/COTS DIGEST*** magazine and will be folding that publication into *MES* over the next couple of months. Our circulation will expand to around 35,000 (print) and 25,000 electronic. No need to give your copy away anymore.

We'll also start a new section in *Military Embedded Systems* called *MIL/COTS DIGEST* ***New Products*** so we can make you aware of the literally hundreds of new COTS products that suppliers announce every month. In addition, we've purchased the mailing list of the **GSPx DSP trade show** and will use this information to broaden several of our magazines including **DSP-FPGA.com,** ***VME and Critical Systems***, plus sister publication ***Embedded Computing Design.*** For you readers, we're "bulking up" on myriad new technologies in microprocessors, FPGAs, DSP, and software. We think you'll find our magazines – print and electronic – more valuable than ever over the next several months.



Chris A. Ciufo
Group Editorial Director

To read more commentary by Chris Ciufo, check out www.vmenow.com.

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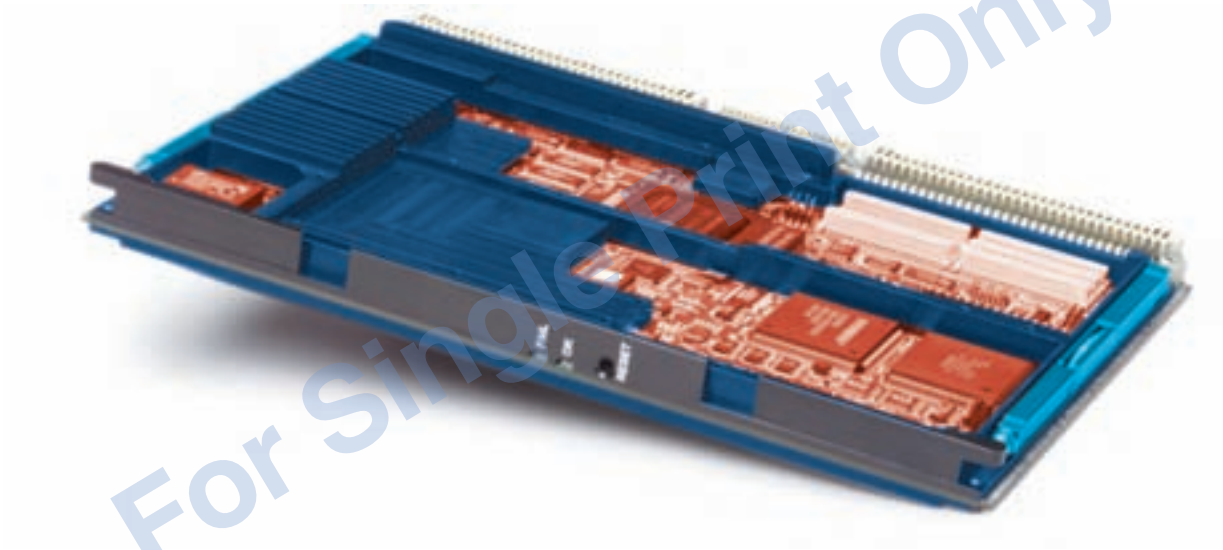
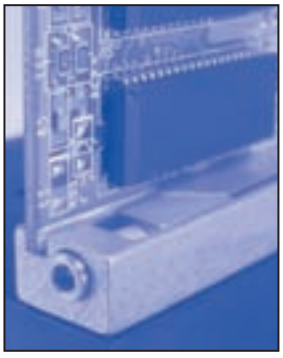


Wedge-Tainer™



- Designed to comply with MIL-STD-810D and MIL-STD-901D in addition to MIL-E-5400

Wedge-Lok®

- Meets the requirements of drawing 84103, Defense Supply Center, Columbus

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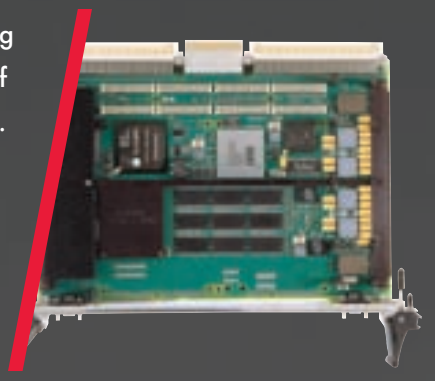


Ruggedization Levels

Spec	Air-cooled Level 0	Air-cooled Level 50	Air-cooled Level 100	Air-cooled Level 200 (Note 5)	Conduction-cooled Level 100	Conduction-cooled Level 200	Conduction-cooled Level 300 (Note 5)
Operating Temperature	0°C to 50°C (Note 6)	-20°C to 65°C (Note 6)	-40°C to 71°C (Note 6)	-40°C to 85°C (Note 6)	-40°C to 71°C (Note 7)	-40°C to 85°C (Note 7)	-40°C to 85°C (Note 7)
Non-Oper. Temperature (Storage)	-40°C to 85°C	-40°C to 85°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Operating Humidity	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% condensing
Non-Oper. Humidity (Storage)	0 to 95% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing
Vibration Sine (Note 1)	2 g peak 15-2k Hz	2 g peak 15-2k Hz	10 g peak 15-2k Hz	10 g peak 15-2k Hz	10 g peak 15-2k Hz	10 g peak 15-2k Hz	10 g peak 15-2k Hz
Vibration Random (Note 2)	0.01 g^2/Hz 15-2k Hz	0.02 g^2/Hz 15-2k Hz	0.04 g^2/Hz 15-2k Hz	0.04 g^2/Hz 15-2k Hz	0.1 g^2/Hz 15-2k Hz	0.1 g^2/Hz 15-2k Hz	0.1 g^2/Hz 15-2k Hz
Shock (Note 3)	20 g peak	20 g peak	30 g peak	30 g peak	40 g peak	40 g peak	40 g peak
Conformal Coat (Note 4)	No	Consult Factory	Yes	Yes	Yes	Yes	Yes
2 Level Maintenance Ready	-	-	-	-	No	No	Yes

Notes

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Conformal coating type is manufacturing site specific.*
5. This is a non-standard product.*
6. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow.*
7. Temperature is measured at the card edge.

*Consult the factory for details.

6U PowerPC SBCs

Product	Form-Factor	Processor(s)	SDRAM/ DDR	Flash	NVRAM	PMC sites	Serial I/O	USB	Ethernet	Rugged-ization	O/S	Other
185	6U VPX /VPX-REDI	Dual-core 8641	2 GB DDR II	512 MB	128 KB	1x64-bit/ 100MHz or 8-lane PCIe, 1x64-bit/66MHz or 4-lane PCIe	4x RS-232, 4x RS-232/ 422/485	2 x USB 2.0	4 x GbE	AC 0,100, CC 100,200 CC VITA 48.2 Type I	VxWorks	SRIO and PCIe back-plane fabric, 2 x 1553B, dual SATA option, SCSI option, 5V-only
184	6U VME	Dual-core 8641	2 GB DDR II	512 MB	128 KB	1x64-bit/ 100MHz or 8-lane PCIe, 1x64-bit/ 66MHz	2x EIA-232, 4x EIA-422/485	2x 2.0	3 x GbE	AC 0,100 CC 100,200	VxWorks	Dual 1553B option, Dual SATA option, SCSI option, 5V-only
183	6U VME	Single/Dual 7447A/7448 1.0/1.2 Ghz	2GB DDR	512 MB	128 KB	1x 64-bit/ 100MHz 1x 64-bit/ 66MHz	2x EIA-232 4x EIA-422/485	2x 2.0	2x GbE 1 x 10/100 Mbps	AC 0,100 CC 100,200	INTEGRITY Linux LynxOS VxWorks	Dual 1553B option, Dual Serial ATA option, SCSI option, 5V-only operation
MANTA DX3	6U VME320	Single/dual PPC 7457 733MHz to 1.3GHz	2GB DDR	64 MB (NOR) 1 GB (NAND)	128 KB	1x 64-bit/ 33 MHz 1x 64-bit/ 133 MHz	4x EIA-232/422/ 485	-	2x GbE	AC 0,50,100	INTEGRITY Linux VxWorks	2x StarFabric links, 2x Serial ATA option
182	6U VME	Single/Dual 7457 1.0 GHz	1GB DDR	128MB	128KB	1x 64-bit/ 100MHz	2x EIA-232 4x EIA-422/485	2x 2.0	2x GbE	AC 0,100 CC 100,200	INTEGRITY TimeSys Linux VxWorks	Dual 1553B option, 5V-only operation
RAPTOR DX2	6U VME	Single/dual PPC 7457 733MHz to 1.3GHz	1GB	128 MB	128 KB	2x 64-bit 33/66 MHz	4x EIA-232/422/ 423	_	3x 10/100 Mbps	AC 0,50,100	INTEGRITY Linux VxWorks	2x StarFabric links 2x FireWire
RHINO DX	6U VME	Single/dual PPC 7457 733MHz to 1.3GHz	1GB	64 MB (NOR) 1 GB (NAND)	128 KB	2x 64-bit/ 66 MHz	4x EIA-232/422/ 423	-	2x 10/100 Mbps	CC 100, 200	INTEGRITY Linux VxWorks	2x FireWire
RAPTOR GX	6U VME	Single PPC 7457 733MHz to 1.3GHz	1GB	128 MB	128 KB	2x 64-bit 33/66 MHz	4x EIA-232/422/ 423	2 x 1.1	3x 10/100 Mbps	AC 0,50,100	INTEGRITY Linux VxWorks	Video/ Graphics 2x FireWire, 1x Ultra160 SCSI option
RAPTOR MX	6U VME	Single/dual PPC 7457 733MHz to 1.3GHz	1GB	64 MB (NOR) 512 MB (NAND)	128 KB	1x 64-bit/ 66 MHz 1x 64-bit/ 33 MHz	4x EIA-232/422/ 485	2 x 2.0	3x 10/100 Mbps	AC 0,50,100	INTEGRITY Linux VxWorks	2x MIL-STD-1553 2x FireWire

Products Continued on Next Page.

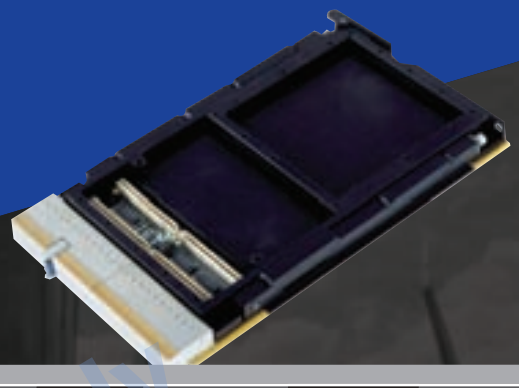
6U PowerPC SBCs

Products Continued From Previous Page.

Product	Form-Factor	Processor(s)	SDRAM/ DDR	Flash	NVRAM	PMC sites	Serial I/O	USB	Ethernet	Rugged-ization	O/S	Other
RHINO MX	6U VME	Single/dual PPC 7457 733MHz to 1.3GHz	1GB	64 MB (NOR) 512 MB (NAND)	128 KB	1x 64-bit/ 66 MHz 1x 64-bit/ 33 MHz	6x EIA-232/422/ 485	2 x 2.0	2x 10/100 Mbps	CC 100, 200	INTEGRITY Linux VxWorks	2x MIL-STD-1553 2x FireWire
181	6U VME	7410 500MHz	1GB	128MB	32KB	1x 64-bit/66MHz 1x 64-bit/ 33MHz	2x EIA-232 4x EIA-422/485	2 x 1.1	2x 10/100 Mbps	AC 0,100 CC 100,200	INTEGRITY LynxOS TimeSys Linux VxWorks	5V-only operation
RHINO 10	6U VME	Single/Dual 7410 466MHz	1GB SDRAM	64MB (NOR)	128KB	2x PMC 64bit/ 66MHz	4x EIA-232 /422/423	-	1x 10/100 Mbps	CC 100, 200	INTEGRITY Linux VxWorks	2x StarFabric option, 2x Firewire
179	6U VME	750/7400 400MHz	256MB	48MB	32KB	2x 64-bit/ 33MHz	2x EIA-232 2x EIA-422/485	-	1x10/100 Mbps	AC 0,100, 200 CC 100,200	INTEGRITY LynxOS TimeSys Linux VxWorks	5V-only operation
FALCON 10	6U VME	Single/Dual 7410 500MHz	1GB SDRAM	64MB (NOR)	128KB	2x PMC 64bit/ 66MHz	4x EIA-232 /422/423	-	3x 10/100 Mbps	AC 0, 50	INTEGRITY Linux VxWorks	2x Firewire
COUGAR 10	6U VME	Single/Dual 7410 500MHz	512MB SDRAM	64MB (NOR)	128KB	1x64 bit/ 33MHz	2x EIA-232 /422/423	-	1x 10/100 Mbps	AC 0, 50	Linux VxWorks	1x Ultra-wide SCSI

6U Intel Processor Based SBCs

Product	Form-Factor	Processor(s)	SDRAM/ DDR	Flash	NVRAM	PMC sites	Serial I/O	USB	Ethernet	Ruggedization	Operating System Support	Other
SVME/ DMV-1901	6U VME	Intel Core-Solo/ Duo @ 1.67/2.0 GHz	2GB DDR2 SDRAM	4 GB USB NAND	-	1x 64bit/ 66MHz & 1x 64 bit/ 133MHz or XMC Sites: 2x 8xPCI express	2x EIA-232, 4x EIA-422	3x USB 2.0	2x GbE	AC 0,50,100 CC 100,200	VxWorks, Solaris, Windows, Linux	2x SATA, 2x SCSI 320/160, 1x VGA Graphics, 1x AC97 Audio
PMA	6U VME	Pentium M 1.4 GHz	Up to 1GB	128MB	32KB	1x 64-bit/ 66MHz	2x EIA-232 2x EIA-422/485	2 x USB 2.0	2x 10/100/1000 BaseT X Ethernet ports	AC 0,100 CC 100,200	Linux VxWorks Solaris	Integrated Graphics, DVO



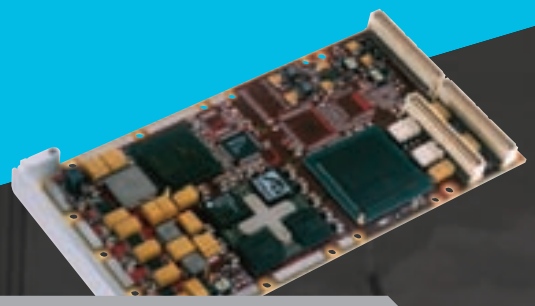
Small Form-Factor SBCs

Product	Form-Factor	Processor	SDRAM/ DDR	Flash	NVRAM	PMC sites	Serial I/O	USB	Ethernet	Rugged-ization	Operating System Support	Other
SCP/DCP-1201	3U cPCI	Intel Core-Solo/Duo @ 1.67 GHz	1 GB DDR2 SDRAM	2 GB USB NAND	-	1x 64bit/ 66MHz	2x EIA-232 4x EIA-422	3x USB 2.0	2x GbE	AC 0,50,100 CC 100,200	VxWorks, Solaris, Windows, Linux	System & Peripheral Controller, 1x Rear XMC Site (AC only) w/8xPCI express, 1x Serial ATA
SCP/DCP-124	3U cPCI	7447A @ 1.0MHz or 7448 @ 1.2GHz	1024MB	256MB	128KB	1x 64-bit/ 100MHz	2x EIA-232 2x EIA-422/485	1 x USB 2.0	2x GbE	AC 0,100 CC 100,200	VxWorks Linux	System & Peripheral controller
SCP/DCP-122	3U cPCI	750FX 800MHz	256MB	64MB	32KB	1x 64-bit/ 66MHz	1x EIA-232 2x EIA-422	1 x USB 1.1	1x 10/100 Mbps	AC 0,100 CC 100,200	INTEGRITY VxWorks Linux	System & Peripheral controller
PMC-106	PPMC	7447A 500MHz	256/ 512MB DDR	64MB	8KB	1x 64-bit/ 66MHz	2x EIA-232/422	-	1x GbE	AC 0,100 CC 100,200	VxWorks Linux	PCI-X 133MHz interface
X/PMC-110 Kryptonite	PMC or XMC	8555e 667 MHz	64MB DDR (expand-able)	16MB	2Mb	-	1xEIA232	-	2x GbE	AC 0,100 CC 100,200	VxWorks Linux	Contact Factory: 64-bit PCI-X 133MHz Interface, Crypto Engine (AES, 3DES, MD5, SHA), Firewall, VPN, NAT, IPSec, IPv4/v6, Random number generators, SNTP, Real-Time Clock

Product	Form-Factor	Proces-sor(s)	Memory	Flash (Max)	NVRAM	Mezz-anine sites	Ethernet	Rugged-ization	O/S	EIA-232 ports	EIA-422/ 485 ports	Discrete I/O	Other Features
CHAMP-AV6	6U VPX-REDI	quad 8641/ 8641D 1GHz/ 1.33GHz	4GB DDR2 (ECC)	512MB	128KB	1x XMC (PCIe)	4 x GbE via switch	AC 0,100 CC 100,200	Linux, VxWorks	4	2	16-bits	SRIO fabric, PCIe I/O port
CHAMP-AV IV	6U VME	quad 7447/7448 1GHz/ 1.25GHz	512MB DDR (ECC)	256MB	128KB	64-bit/ 100 MHz	4 x GbE via switch	AC 0,100 CC 100,200	INTEGRITY, Linux, VxWorks, Gadae	4	-	8-bits	On-board Gigabit Ethernet Switch
CHAMP-FX2	6U VPX-REDI	Two Xilinx Virtex 5 FPGAs, LX110T/ LX330T. One 8641D	(Note 1)	256 MB	-	1x XMC (PCIe)	10/100/ 1000 Mbps	AC 0, 100 CC 100,200	Linux, VxWorks	2	2	16-bits	SRIO fabric (six x4 ports offboard), two Serial RocketIO ports to backplane
CHAMP-FX	6U VME	dual Xilinx VP-70/100	512MB DDR 36MB SDRAM	128MB	-	2x 64-bit/66 MHz	-	AC 0,100, CC 100,200	-	1	-	-	2 x StarFabric Links, FPGA design kit, VITA 41, VME64x versions
Manta QX3	6U VME	quad 7457 733MHz/ 1GHz	2GB DDR	64MB (NOR) 1GB (NAND)	128KB	1x 64-bit/ 66 MHz	2x 10/100/ 1000 Mbps	AC 0,50	INTEGRITY, Linux, VxWorks	4	2	12-bits	2 x StarFabric Links, 2x FireWire
Manta QX3 (Note 2)	6U cPCI, PICMG 2.16	quad 7457 733MHz/ 1GHz	2GB DDR	64MB (NOR) 1GB (NAND)	128KB	1x 64-bit/ 66 MHz	2x 10/100/ 1000 Mbps	CC 100,200	INTEGRITY, Linux, VxWorks	4	2	-	2 x StarFabric Links, 2x FireWire

Notes

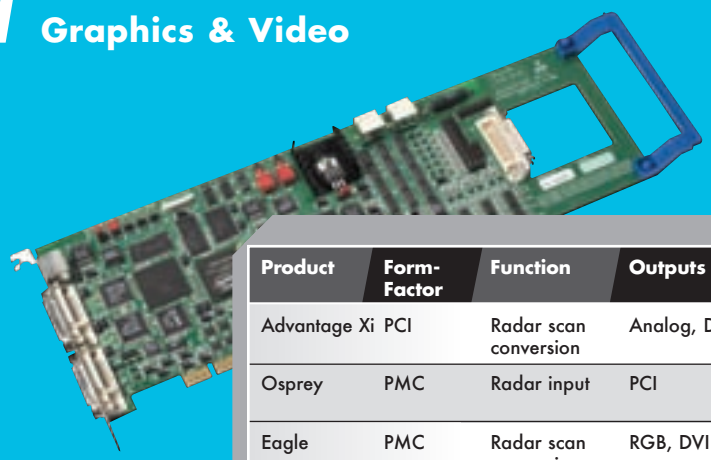
1. 512 MB DDR2 SDRAM, 72 MB QDR SDRAM per FPGA. 512 MB DDR2 SDRAM for the PowerPC
2. Manta QX3 PMC operates at 66MHz if StarFabric option is selected.



Product	Form-Factor	Graphics Processor	Inputs				Outputs					Software API – Operating System	Ruggedization	Other
			RGB	NTSC/ PAL/ RS-170	LVDS	DVI	RGB	NTSC/ PAL/ RS-170	RS-170/ RS-343/ STANAG 3350	LVDS	DVI			
PMC-704	PMC	ATI M9	1	4	1	-	2	1	1	2	2	OpenGL/X11 VxWorks/INTEGRITY	AC 0,100 CC 100,200	External Sync (Note 1)
PMC-706	PMC	ATI M9	-	-	-	-	2	1	-	2	2	OpenGL/X11/Windows VxWorks/INTEGRITY	AC 0,100 CC 100,200	(Note 1,2)
PMC-724	PMC	None	-	4	1	-	-	-	-	-	-	VxWorks/INTEGRITY	AC 0,100 CC 100,200	Frame Grabber
Raptor GX	6U VME	-	-	-	-	-	1	-	-	-	1	VxWorks, Linux	AC 0,100	SBC with graphics
Atlas	PMC	ATI M9	1	1	-	1	2	2	-	-	2	X11/OpenGL/SDL/WindML/ DirectX/Solaris/Linux/ VxWorks/LynxOS/Windows	AC 0,100	Includes USB and Audio I/O RoHS vers Q106
Sabre-G	6U VME	ATI M9 (x2)	-	-	-	-	2	-	-	-	2	X11/Linux/Solaris/ LynxOS	AC 0, 50	Sabre graphics with underlay/ overlay architecture
Sabre-V	6U VME	ATI M9 (x2)	2	8	-	2	2	-	-	-	2	X11/Linux, Solaris/ LynxOS	AC 0, 50	Sabre graphics video capture, high-quality scaling and windowing with multilayer architecture

Notes

1. Not all input/output combinations are available in all variants. Refer to the datasheet for greater detail or contact your sales representative.
2. A DO-178B driver can be made available for this item. Please contact your sales representative.



Radar Acquisition, Processing and Scan Conversion

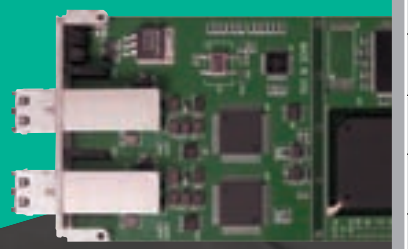
Product	Form-Factor	Function	Outputs	Inputs	Software API – Operating System	Ruggedization	Other
Advantage Xi	PCI	Radar scan conversion	Analog, DVI	DVI from graphics card	Windows, Linux, Solaris, LynxOS	AC 0	Radar scan conversion with underlay/overlay via DVI-D input
Osprey	PMC	Radar input	PCI	3 analog, 3 digital, ACP/ARP, serial or parallel formats	Windows, Linux, Solaris, LynxOS	AC 0	Radar input 50MHz 10-bit ADC or digital input
Eagle	PMC	Radar scan conversion	RGB, DVI	PCI, DVI-D	Windows, Linux, Solaris, LynxOS	AC 0 CC 100	Radar scan conversion with underlay/overlay via DVI-D input
Osiris	PMC, PCI	Radar input	PCI	Radar inputs: 2 analog radar videos, 8 digital radars, 2 triggers, 2 sets of turning data	Windows, Linux	AC 0	High-performance dual-channel radar interface card
Advantage Zeta	PCI	Radar input scan conversion	RGB, DVI	Radar inputs: 3 Analog, 3 digital, ACP/ARP, serial or parallel	Windows, Linux, Solaris, LynxOS	AC 0	Combined radar input and scan conversion
Sabre-R	6U VME	Graphics and radar scan conversion	2 x DVI-I	Radar input: Via RVP Server Video inputs: 2 x RGB, 2 x DVI-D, 8 x TV	Linux, Solaris, LynxOS	AC 0	Combined graphics, video windows and radar scan-converter module
RVP Radar Distribution	VME, cPCI or turnkey system	Radar distribution	Radar video data on LAN	Radar inputs	Windows, Linux, Solaris	AC 0, 50	Radar video distribution on LAN
RVP Radar Tracker	VME, cPCI or turnkey system	Radar tracker	Radar video plot or track data on LAN	Radar inputs or external plot input	Windows, Linux, Solaris	AC 0, 50	Radar video plot extractor and tracker

Video Distribution, Windowing and Recording

Product	Form-Factor	Function	Outputs	Inputs	Ruggedization
Cobra	6U VME	4 video windows, scaled and positioned. Video overlay, video cross-mixing, alpha blending	RGB, DVI	12x RGB, TV, RS170, RS343 1x DVI	AC 0, 50 (Note 1)
VxPoint	6U VME	Video crosspoint switch	32x RGB, NTSC, PAL	8x RGB, NTSC, PAL	AC 0 Note 1
Orion JPEG2000	PMC, PCI	JPEG 2000 compression/ decompression	2x TV, PCI	10x TV, PCI	AC 0
Sentric Recorder	VME, Desktop, Rackmount	Digital screen recording system	4x RGB, 2x DVI 4x audio, 4x TV	4x RGB, 2x DVI 4x audio, 4x TV	AC 0
Video Buffer	VME	RGB buffer. Each of two RGB inputs is split and buffered to two RGB outputs.	4x RGB	2x RGB	AC 0
Sabre-V	6U VME	Combined graphics and dual video windows processor	2 x DVI-I	2 x RGB, 8 x TV, 2 x DVI-D	AC 0, 50

Note 1: Ruggedized version available, consult your sales representative.

High Performance Communications Products



Product	Form-Factor	Interface type and number	Speed	Operating System/ Protocol Support	Ruggedization	Other
PMC-643	PMC	2 Fibre Channel	2.125 Gbps	VxWorks VI/IP/SCSI	AC 0,100 CC 100,200	Onboard hub. Supports copper interface through backplane connectors
FX400	PMC	1 Fibre Channel	4.250, 2.125, 1.0625 Gbs	Linux, VxWorks, Window	AC 0,100	133 MHz PCI-X, multi-protocol driver
FX400	PMC	2 Fibre Channel	4.250, 2.125, 1.0625 Gbs	Linux, VxWorks, Windows	AC 0,100	133 MHz PCI-X, multi-protocol driver
StarLink II	PMC	4 StarFabric ports	440MB/s total	VxWorks, INTEGRITY, Linux	AC 0,100 CC 100,200	Includes integrated StarFabric switch
PSTB	PMC	2 StarFabric ports (Bridge Only)	2.5 Gbps	VxWorks, Linux	AC 0,100 CC 100,200	-
PSTN	PMC	2x Star Fabric Ports (Bridge and Switch)	2.5 Gbps	VxWorks, Linux	AC 0, 50, 100 CC 100, 200	-
FibreXtreme SL100	PMC	Serial FPDP (Note 1)	1.0625 Gbps 105MB/s throughput	Linux, Solaris, VxWorks	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL100	PCI	Serial FPDP (Note 1)	1.0625 Gbps 105MB/s throughput	IRIX, Linux, Solaris, VxWorks, Windows	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL100	cPCI	Serial FPDP (Note 1)	1.0625 Gbps 105MB/s throughput	VxWorks, Windows	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL100	CMC (Note 5)	Serial FPDP (Note 1)	1.0625 Gbps 105MB/s throughput	-	AC 0 (Note 2)	Extends FPDP up to 50km; several carrier options available – VME and PCI (Note 3)
FibreXtreme SL240	PMC	Serial FPDP (Note 1)	2.5 Gbps 247MB/s throughput	Linux, Solaris, VxWorks	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL240	PCI	Serial FPDP (Note 1)	2.5 Gbps 247MB/s throughput	IRIX, Linux, Solaris, VxWorks, Windows	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL240	cPCI	Serial FPDP (Note 1)	2.5 Gbps 247MB/s throughput	VxWorks, Windows	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL240	CMC (Note 5)	Serial FPDP (Note 1)	2.5 Gbps 247MB/s throughput	-	AC 0 (Note 2)	Extends FPDP up to 50km; VME & PCI carrier options
FibreXtreme SL100DC (Note 6)	XMC PCIe	Serial FPDP (Note 1)	1.0625 Gbps 105 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL100DC (Note 6)	PCI PCIe	Serial FPDP (Note 1)	1.0625 Gbps 105 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL240DC (Note 6)	XMC PCIe	Serial FPDP (Note 1)	2.5 Gbps 247 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL240DC (Note 6)	PCI PCIe	Serial FPDP (Note 1)	2.5 Gbps 247 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2)	Extends FPDP up to 50km

Products Continued on Next Page.

High Performance Communications Products

Products Continued From Previous Page.

Product	Form-Factor	Interface type and number	Speed	Operating System/ Protocol Support	Ruggedization	Other
FibreXtreme SL100QC (Note 7)	XMC PCIe	Serial FPDP (Note 1)	1.0625 Gbps 105 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL100QC (Note 7)	PCI PCIe	Serial FPDP (Note 1)	1.0625 Gbps 105 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2)	Extends FPDP up to 50km
FibreXtreme SL240QC (Note 7)	XMC PCIe	Serial FPDP (Note 1)	2.5 Gbps 247 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Extends FPDP up to 50km
FibreXtreme SL240QC (Note 7)	PCI PCIe	Serial FPDP (Note 1)	2.5 Gbps 247 MB/channel	VxWorks, Windows, Linux	AC 0 (Note 2)	Extends FPDP up to 50km
SCRAMNet+ SC150e	PCI	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	250nsec latency
SCRAMNet+ SC150e	cPCI	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	250nsec latency
SCRAMNet+ SC150e	PMC	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	250nsec latency
SCRAMNet+ SC150	PCI	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	250nsec latency
SCRAMNet+ SC150	VME	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	250nsec latency
SCRAMNet+ SC150	3.3" x 4.0"	Shared Memory (Note 8)	150 Mbps 16.7MB/s throughput	VxWorks, HP UX, QNX, Windows, Linux, IRIX, Solaris	AC 0 (Note 2)	Mezzanine for rehosting onto custom carrier
SCRAMNetGT GT200	PCI	Shared Memory (Note 9)	2.5Gbps 200MB/s throughput	Windows, Linux, IRIX, VxWorks, Solaris, RTX, MATLAB, LabView	AC 0 (Note 2)	Memory options starting at 128MB
SCRAMNetGT GT200	PMC	Shared Memory (Note 9)	2.5Gbps 200MB/s throughput	Windows, Linux, IRIX, VxWorks, Solaris, RTX, MATLAB, LabView	AC 0 (Note 2) AC 200 (Note 3) CC 200 (Note 4)	Memory options starting at 128MB
SCRAMNetGT GT200	VME	Shared Memory (Note 9)	2.5Gbps 210MB/s throughput	Windows, Linux, IRIX, VxWorks, Solaris, RTX, MATLAB, LabView	AC 0 (Note 2)	Memory options starting at 128MB
PGE2	PMC	2 X Gb Ethernet	1 Gb/s	VxWorks, Linux	AC 0,50,100 CC 100,200	Front or rear I/O
PEF2	PMC	2 X 100BaseFx Ethernet	100 Mb/s	VxWorks, Linux	AC 0,50,100	-
PSCR	PMC	1 X Ultra160 SCSI	160 MB/s	VxWorks, Linux	CC 100,200	-
PSC2	PMC	2 X Ultra160 SCSI	160 MB/s	VxWorks, Linux	AC 0,50,100	1 ea. Front and rear I/O
PFIR	PMC	2 X FireWire (IEEE 1394)	400 Mb/s	VxWorks, Linux	AC 0,50,100 CC 100,200	-

Notes

1. FibreXtreme Serial FPDP products are available with copper or 800nm/1300nm/1550nm optical transceivers.

2. Humidity 10% to 85% non-condensing, no shock or vibration testing.

3. Storage Temperature -40°C to +85°C, Humidity 0% to 95% Non-condensing.

4. Storage Temperature -40°C to +85°C, Humidity 0% to 95% Non-condensing, Random Vibration .1g^2/Hz 10 Hz to 1k Hz, -6dB/octave 1k Hz to 2k Hz.

5. The CMC format provides a 32-bit parallel interface for conversion to Serial FPDP. FibreXtreme CMC cards can be mounted on companion VME or PCI carrier boards, or used with a custom carrier.

6. FibreXtreme DC products provide 2 independent Serial FPDP channels.

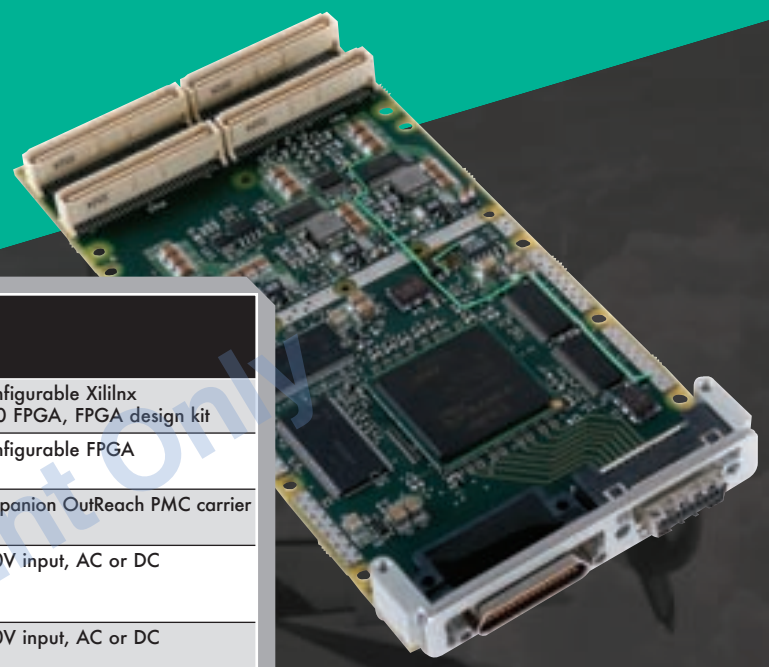
7. FibreXtreme QC products provide 4 independent Serial FPDP channels.

8. SCRAMNet+ is a ring topology shared memory network, available in copper, standard fiber (300M) or extended fiber (3000M) media. Reconfigurable networks can be constructed with use of the optional Curtiss-Wright physical layer switches.

9. SCRAMNet GT is a ring topology shared memory network operating at 2.5Gbps, available in standard fiber (300M) or extended fiber (3000M) media. Reconfigurable networks can be constructed with use of the optional Curtiss-Wright physical layer switches.

Avionics/Vehicle Bus & Serial I/O Communications Products

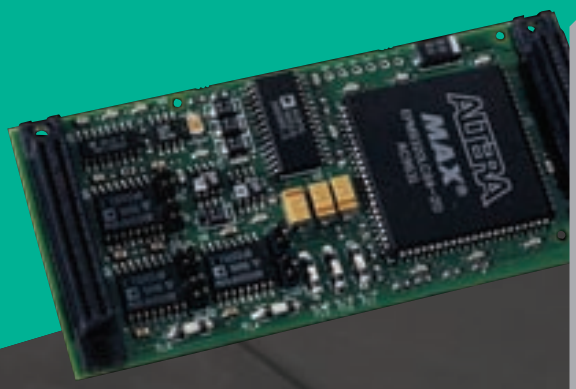
Product	Form-Factor	Interface type and number	Speed	Operating System/ protocol support	Ruggedization	Other
PMC-211	PMC	2 CANbus	250/500, 1000Kbps	VxWorks	AC 0,100 CC 200	Optional US Army Utility bus
P429A	PMC	ARINC-429 (4 Tx, 8 Rx) 12 serial ports	1Mbps	VxWorks	AC 0,100 CC 100,200	4 RS-485/RS-422 serial ports
PMC-601	PMC	2 MIL-STD-1553	1 Mbps	VxWorks, INTEGRITY, LynxOS	AC 0,100 CC 200	16-bit discrete I/O
P1553	PMC	3 MIL-STD-1553	1 Mbps	VxWorks	AC 0,100 CC 100,200	1,2,3 channel versions
1553 Gold+	PC-AT	2 MIL-STD-1553	1 Mbps	Windows	AC 0	Single & multi-mode versions
1553 Gold+	PCI	2 MIL-STD-1553	1 Mbps	Windows, Linux, Solaris	AC 0	Single & multi-mode versions
1553 Gold+	PMC	1 MIL-STD-1553	1 Mbps	Windows, Linux, Solaris, VxWorks	AC 0	Single & multi-mode versions
1553 Gold+	VME	2 MIL-STD-1553	1 Mbps	Unix, SunOS, Solaris	AC 0	Single & multi-mode versions
1553	BIU Express VME	1 MIL-STD-1553	1 Mbps	Unix	AC 0	Single mode
P15D	PMC	2x MIL-STD-1553	1 Mb/s	VxWorks, Linux	AC 0,50,100 CC 100,200	Front or rear I/O
PARD	PMC	4x ARINC 429/575 Tx 8x ARINC 429/575 Rx	High 100 kb/s Low 12.5 kb/s	VxWorks, Linux	AC 0,50,100 CC 100,200	8 GPIO



VME and PMC I/O Products

Product	Form-Factor	I/O interface	Operating System Support	Ruggedization	Other
PMC-440	PMC	78 LVTTL or 39 LVDS 8 Rocket I/O	VxWorks	AC 0,100 CC 100,200	User configurable Xililnx VP20/40 FPGA, FPGA design kit
PMC-GPIO	PMC	64 LVTTL or 32 LVDS	VxWorks	AC 0,100 CC 100,200	User configurable FPGA
PMC-605	PMC	PCI to P0	VxWorks	AC 0,200 CC 200	See companion OutReach PMC carrier
CM-DIO-40	VME	opto-isolated digital I/O 32 inputs, 32 relay or opto-isolated outputs	VxWorks	AC 0,100 CC 100,200	3 to 300V input, AC or DC
CM-DI-40	VME	opto-isolated digital I/O 64 inputs	VxWorks	AC 0,100 CC 100,200	3 to 300V input, AC or DC
CM-DO-40	VME	opto-isolated digital I/O 64 outputs	VxWorks	AC 0,100 CC 100,200	Options for relay, opto-coupler, photo MOS, SSR, Triac, SCR, source or sink
CM-DS-40	VME	Digital to synchro/ Resolver 4 or 8 channels	VxWorks	AC 0,100 CC 100,200	16-bit resolution, 200Hz to 1KHz bandwidth
CM-SD-40	VME	Synchro/resolver to digital 16 channels	VxWorks	AC 0,100 CC 100,200	Synchro input: 90 or 11.8V RMS Resolver input: 90, 26 or 11.8V RMS
CM-SDS-40	VME	Synchro/resolver I/O 4 inputs/4 outputs	VxWorks	AC 0,100 CC 100,200	Synchro input: 90 or 11.8V RMS Resolver input: 90, 26 or 11.8V RMS
CM-AD-45	VME	Analog input 32 single-ended, 16 differential	VxWorks	AC 0,100 CC 100,200	12-bit resolution, 0-5V, 0-10V, 0-50V, 0-100V inputs
CM-DA-50	VME	Analog output 24 outputs	VxWorks	AC 0,100 CC 100,200	14-bit resolution, 0-5V, 0-10V, ±5V, ±10V, 20mA outputs

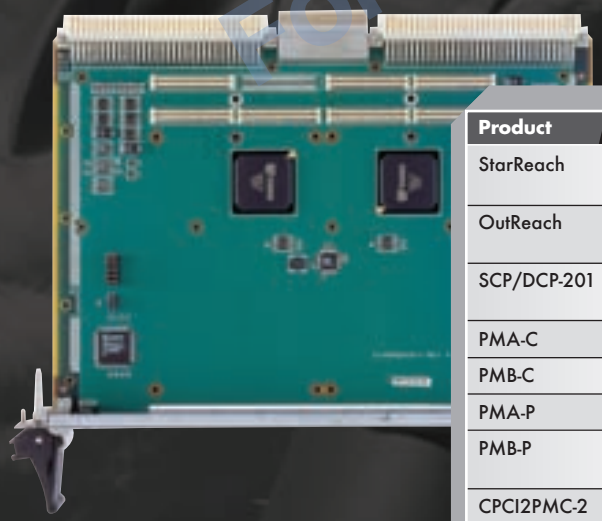
IndustryPack® I/O Modules



Product	I/O interface	Operating System Support	Ruggedization	Other
IP4-206	Opto-isolated digital I/O 16 input/outputs or 24 inputs	VxWorks	AC 0,100 CC 100,200	MIL-STD-704, MIL-STD-1275 compliant input/output
IP4-660	Analog input 16 single-ended or 8 differential	VxWorks	AC 0,100 CC 100,200	16-bit resolution ±10V, ±5V, +10V, +5V ranges
IP4-661	Analog output 3 outputs	VxWorks	AC 0,100 CC 100,200	16-bit resolution ±10V, ±5V, +10V, +5V ranges
ADC128F1	Analog input 8 channel	OS-9, Windows	AC 0	12-bit resolution, ±10V range
ADM1224F	Analog input 24 channel	OS-9, Windows	AC 0	Triple ADC converter, multiplexed differential inputs
DAC128F5	Analog output 8 channels	OS-9	AC 0	12-bit resolution, ±5V range
DAC128V	Analog output 8 channels	OS-9, Windows	AC 0	12-bit resolution, 8 voltage ranges
DIO316I	Digital I/O 16 inputs 16 outputs 16 I/O	OS-9, Windows	AC 0	Interrupt on input change
TRIDO48	Digital output 48 channels	OS-9, Windows	AC 0	Tristatable outputs
OPTDO32	Opto-isolated digital output 32 channels	OS-9	AC 0	3000V isolation, open collector with pull-ups
DID48	Digital input 48 channel	OS-9, Windows	AC 0	Hardware de-bounced inputs, interrupt on change
LOW40	High power driver 40 channel	OS-9, Windows	AC 0	Low side open collector outputs, transient protected
RELAY16	Relays 16 Form C	OS-9, Windows	AC 0	1A relays, integrated transient suppression
REED25	Relays 25 Reed	OS-9, Windows	AC 0	Magnetically shielded relays for EMI sensitive applications
COMM232	Serial I/O 4 EIA-232 ports	OS-9	AC 0	Full handshaking signals
DUAL32CT	Counter/Timer dual 32-bit	OS-9, Windows	AC 0	Clock generation, watchdog timers, variable period/duty cycle generation

IndustryPack® Carrier Cards

Product	Form-Factor	IP sites	Ruggedization	Other
215 Carrier Express	6U VPX	2 X/PMC sites + 1 IPM site	AC 0,100 CC 100,200	VITA 46.0 compliant, 4xPCIe ports on P1, I2C manageable, rear panel I/O
216 Carrier Express	3U VPX	1 X/PMC site	AC 0,100 CC 100,200	Contact Factory. VITA 46.0 compliant, 4xPCIe ports on P1, I2C manageable, rear panel I/O
SVME/DMV-209	VME	4	AC 0,100 CC 100,200	Rear panel I/O, onboard 15V PSU
VMESC5	VME	5	AC 0	Up to 250 I/O points per slot
ISASC6	ISA	6	AC 0	Up to 200 I/O points per slot
ISASC6	PCI	3	AC 0	Up to 150 I/O points per slot
PCISC5	PCI	5	AC 0	Up to 250 I/O points per slot



PMC Carrier Cards

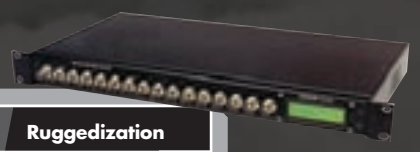
Product	Form-Factor	PMC interface	Ruggedization	Other
StarReach	6U VME	2x 64-bit/66MHz	AC 0,100 CC 100	StarFabric interface extends PCI to 5M
OutReach	6U VME	2x 32-bit/33MHz	AC 0,200 CC 200	Companion PMC-605 PCI to P0
SCP/DCP-201	3U cPCI	1x 64-bit/66MHz	AC 0,100 CC 100,200	-
PMA-C	3U cPCI	1x 64-bit/66MHz	AC 0,100	-
PMB-C	6U cPCI	2x 64-bit/66MHz	AC 0,100	PCI to PCI bridge, hot swap, Pn4 I/O
PMA-P	PCI (short)	1x 64-bit/66MHz	AC 0,100	-
PMB-P	PCI (short)	1x 64-bit/66MHz	AC 0,100	PCI to PCI bridge, SDL and Peritool software support (Frequency & Temp. sensor)
CPCI2PMC-2	6U cPCI	2x 32-bit/33MHz	AC 0,100	PCI to PCI bridge, optional rear panel I/O
PBX3	6U	3 X 32/64-BIT 33/66 MHz	AC 0,50	PCI-to-PCI Bridge, Up to 1 GB SDRAM, Up to 1 GB NAND Flash, Stacking architecture
PEX2	6U	2 X 64-BIT 33 MHz	AC 0,50	Up to 512 MB SDRAM, Up to 128 MB NOR Flash, Stacking architecture

Gigabit Ethernet Switches/Routers

Product	Form-Factor	Port Options	Interface	Software	Ruggedization
PGR8	PMC	8 ports	10BaseT, 100BaseTX, 1000BaseT	Unmanaged (Layer 2 only)	AC 0
650 (rugged PGR8)	PMC	8 ports	10BaseT, 100BaseTX, 1000BaseT	Unmanaged (Layer 2 only)	AC 100 CC 100, 200
671 SwitchExpress	6U VPX	4 PCIe + 8 or 16 GbE	PCIe x4, 10BaseT, 100BaseTX, 1000BaseT	Management interface (PCIe Switch) + Unmanaged (Layer 2 only GbE switch)	AC 0, 100 CC 100, 200
672 SwitchExpress	3U VPX	4 PCIe + 8 or 16 GbE	PCIe x4, 10BaseT, 100BaseTX, 1000BaseT	Management interface (PCIe Switch) + Unmanaged (Layer 2 only GbE switch)	AC 0, 100 CC 100, 200
672 SwitchExpress	3U VPX	8 PCIe	PCIe x4	Contact Factory: Managed interface (PCIe Switch)	AC 0, 100 CC 100, 200
680 SwitchBlade	6U VME	12 or 20 ports	10BaseT, 100BaseTX, 1000BaseT	Managed (Layer 2/3+, IPv4/v6, Multicast, QoS, Security, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
680 SwitchBlade	6U VME	24 ports (20xGbE + 4xGbE or 4xFE or 4xFO-SX)	10BaseT, 100BaseTX, 1000BaseT, 1000BaseSX	Managed (Layer 2/3+, IPv4/v6, Multicast, QoS, Security, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
681 Compact SwitchBlade	3U CPCI	10 ports	10BaseT, 100BaseTX, 1000BaseT	Managed (Layer 2/3+, IPv4/v6, Multicast, QoS, Security, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
683 Compact FireBlade	3U VPX	14 ports (12xGbE + 2x10G XAUI)	10BaseT, 100BaseTX, 1000BaseT, XAUI	Contact Factory: Unamanged, Managed, Security	AC 0, 100 CC 100, 200
682 FireBlade	6U VME	12 ports	10BaseT, 100BaseTX, 1000BaseT	Unmanaged (Layer 2+) OR Managed (Layer 2/3+, IPv4/v6, Multicast, QoS, Security, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
682 FireBlade+ Kryptonite	6U VME	18 ports (12xGbE + 4xFO-SX + 2x10GbE)	10BaseT, 100BaseTX, 1000BaseT, 1000BaseSX, 10G XAUI	Managed + Security (Layer 2/3+, IPv4/v6, Multicast, QoS, Enhanced Security w/ Kryptonite, Firewall, NAT, VPN, IPSec, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
682 FireBlade+ Kryptonite	6U VME	20 ports	10BaseT, 100BaseTX, 1000BaseT	Unmanaged OR Managed + Security (Layer 2/3+, IPv4/v6, Multicast, QoS, Enhanced Security w/ Kryptonite, Firewall, NAT, VPN, IPSec, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
682 FireBlade+ Kryptonite	6U VME	26 ports (20xGbE + 4xFE OR 4xGbE OR 4xFO-SX + 2x10GbE)	10BaseT, 100BaseTX, 1000BaseT, 1000BaseSX, 10G XAUI	Managed + Security (Layer 2/3+, IPv4/v6, Multicast, QoS, Enhanced Security w/ Kryptonite, Firewall, NAT, VPN, IPSec, "De-class" secure memory erase)	AC 0, 100 CC 100, 200
682 FireBlade	6U VPX	26 ports (20xGbE + 4xFE OR 4xGbE OR 4xFO-SX + 2x10GbE)	10BaseT, 100BaseTX, 1000BaseT, 1000BaseSX, 10G XAUI	Contact Factory: Unmanaged, Managed, Security	AC 0, 100 CC 100, 200
SMS-680 SwitchBox	Standalone w/ power supply	12 or 20 ports	10BaseT, 100BaseTX, 1000BaseT	Managed (Layer 2/3+, IPv4/v6, Multicast, QoS, Security, "De-class" secure memory erase)	CC 100, 200
68x RTM	6U VME, CPCI, or VPX	up to 24 ports + 1 debug port + 1 serial port	10BaseT, 100BaseTX, 1000BaseT, RS232	Used with 68x for lab environment	AC 0
68x SW Maintenance	n/a	n/a	n/a	yearly 68x software maintenance	n/a

Note: Switches and Routers with other port and security combinations are also available, please contact factory.

MIL-STD-1553 Switches



Product	Form-Factor	Interface type	Number of ports	Port Options	Ruggedization
MBX1553	19" 1U rack	MIL-STD-1553 A/B	16 LRU and 16 Bus	1553-type transformer coupled	AC 0

Physical Layer Switches & Storage Solutions

Physical Layer Switches

Product	Form-Factor	Interface type	Number of ports	Port Options*	Ruggedization
LX1500e	19" 4U rack	Any digital signal up to 1.5 Gb/s	Up to 32, 4 ports per port card	SC-type, SCRAMNet; ST-type FC and GigE	AC 0
LX2500	19" 4U rack	Any digital signal up to 2.5 Gb/s	Up to 32, 4 ports per port card	SFF-type and SFP-type FC, GigE and SFPDP	AC 0
VLX2500	VME slot or 19" 1U rack	Any digital signal up to 3.125 Gb/s	8 ports and 16 ports	SFP-type FC, GigE and SFPDP	AC 0,100 (Note 1)
GLX4000	19" 4U rack or 8U rack	Any digital signal up to 4.25 Gb/s	144 and 288 ports, 48 ports per port card	SFP-type, FC, GigE, and SFPDP; XFP-type 10 Gig FC and 10 GigE; 9-pin 1394B (Firewire)	AC 0
CLX2500	cPCI slot	Any digital signal up to 1 Gb/s	16 ports	Rear IO, FC and GigE	CC 200

Notes

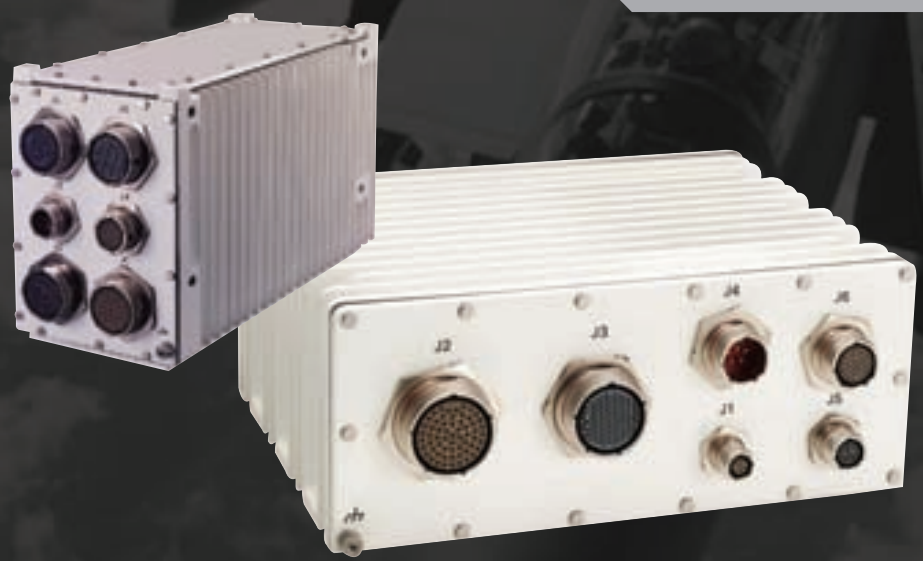
1. Available in -10°C to 70°C air-cooled configuration

FC = Fibre Channel, GigE = Gigabit Ethernet, SFPDP = Serial FPDP

Record/Storage Solutions

Product	Controller Form-Factor	Number of Channels	Storage Options	Ruggedization	Other
SDRxL Streaming Data Recorder	1U Rackmount	1	External 2U Rackmount JBOD with Rotating FC Disks up to 3.6 TB	AC 0	-
	3U Rackmount	2, 4	External 2U Rackmount JBOD(s) with Rotating FC Disks up to 3.6 TB	AC 0	-
SDRxR Streaming Data Recorder	3U Rackmount	1, 2	Integral JBOD with Rotating FC Disks up to 3.6 TB	AC 0, 100	-
EDRxR Event Data Recorder	Custom	1	Integral Solid State Disk up to 128 GB	AC 100, 200	-
PBOD USB NAND Flash	PMC	-	-	AC 0, 50, 100 CC 100, 200	2, 8, 16, 32, and 64 GB 32 bit/66MHz PCI VxWorks, Linux, Windows

Product	Slots	Backplane	Form-Factor	Power Input	Cooling
VPX6-905	6	6U VPX	19" rack	115/230VAC	Air-cooled Internal Fan
OSS-ENCL-3U-5	5	3U cPCI	Bench top	115/230VAC	Air-cooled Internal fan
ATRH-STD	5	6U VME	1/2 ATR Short	28VDC	Conduction-cooled Natural convection
ATRH-STD	5	6U VME	1/2 ATR Short	28VDC	Conduction-cooled Cold plate
3U cPCI chassis	8	3U cPCI	12.62" x 4.88" x 7.62"	28VDC	Conduction-cooled Forced Air
CM-RA-20	5	6U VME	1/2 ATR Long Tall	28VDC or 115VAC	Conduction-cooled Cold plate or forced-air
CM-RA-30	7	6U VME	3/4 ATR Long Tall	28VDC or 115VAC	Conduction-cooled Cold plate or forced-air
ATRS-STD	12	6U VME	1 ATR Short	28VDC or 115VAC	Conduction-cooled Natural convection
ATRS-STD	12	6U VME	1 ATR Short	28VDC or 115VAC	Conduction-cooled Cold plate
CM-RA-40	12	6U VME	1 ATR Long Tall	28VDC or 115VAC	Conduction-cooled Cold plate or forced air
RC-1	1	6U VME or cPCI	12" x 8.25" x 3"	16V to 40 VDC	Conduction-cooled Natural convection
RC-2	2	6U VME	11″ x 4.5″ x 8.5″	28VDC or 115VAC	Conduction-cooled Natural convection
RC-5	5	6U VME	5.8″ x 8.4″ x 14″	28VDC or 115VAC	Conduction-cooled Natural convection



PowerMatrix

PowerMatrix System	Rack type	Processing nodes	Additional cards	Expansion	Memory	Backplane interconnects	Software
SMP 10 / SMP 20	19", 8-slot, air-cooled, VME64x	Manta DX3 (5) or Manta QX3 (5)	PGR8 GigE Switch PSTN StarFabric Bridge/Switch	Up to 5 PMC	10 GB SDRAM, 5 GB Flash	StarFabric, GigE	Global Buffer Manager
SMP 16 / SMP 32	19", 12-slot, air-cooled, VME64x	Manta DX3 (8) or Manta QX3 (8)	20-port GigE Switch PSTN StarFabric Bridge/Switch	Up to 14 PMC	16 GB SDRAM, 8 GB Flash	StarFabric, GigE	Global Buffer Manager
SMP 24 / SMP 48	19", 21-slot, air-cooled, VME64x	Manta DX3 (12) or Manta QX3 (12)	StarBlade Switch (2)	Up to 24 PMC	24 GB SDRAM, 12 GB Flash	StarFabric, GigE	Global Buffer Manager
DSP 1 X 16	19", 8-slot, air-cooled, VME64x	CHAMP-AV IV (4) SVME-183 (1)	StarLink PMC (5)	Up to 5 PMC	4.5 GB SDRAM, 1.25 GB Flash	StarFabric, GigE	Interprocessor Communications Library
DSP 4x16	19", 12-slot, air-cooled, VME64x	CHAMP-AV IV (4) SVME-183 (4)	StarLink PMC (8)	Up to 8 PMC	5 GB SDRAM, 1.25 GB Flash	StarFabric, GigE	Interprocessor Communications Library
DSP 2x12 / 4x12	19", 8-slot, air-cooled, VME64x	CHAMP-AV IV (3) Manta DX3 (2)	StarLink PMC (8) PGR8 GigE Switch PBX3 PMC Carrier (2)	10 PMC	7 GB SDRAM	StarFabric, GigE	Interprocessor Communications Library
DSP 48	19", 21-slot, air-cooled, VME64x	CHAMP-AV IV (12)	StarLink PMC (12)	12 PMC	12 GB SDRAM, 3 GB Flash	StarFabric, GigE	Interprocessor Communications Library
FPGA 1x4x16	19", 8-slot, air-cooled, VME64x	CHAMP-FX (2) CHAMP-AV IV (4) SVME-183 (1)	StarLink PMC (5)	9 PMC	5 GB SDRAM	StarFabric, GigE	Interprocessor Communications Library

- PowerMatrix SMP: Using the proven performance of five Manta dual or quad processor Single Board Computers, PowerMatrix SMP systems fulfill the needs of applications requiring a high level of CPU processing and sharing of data between processing units.
- PowerMatrix DSP: Based on the proven performance of the CHAMP-AV IV DSP computer, PowerMatrix DSP systems are ideally suited for applications that require a high level of CPU processing and high memory bandwidth.
- PowerMatrix FPGA: Built on the performance of the CHAMP-FX compute engine, they can outperform a microprocessor-based system by a factor ten or more using certain signal processing algorithms.

Modular Tactical Computer (MTC)

The MTC is an innovative five-slot 3U CompactPCI (cPCI) system designed for space-constrained platforms. This compact, durable system is constructed from lightweight 6061-T6 aluminum and is equipped with an impressive 130W power supply. The MTC's processing engine is provided by the unmatched, raw compute power of Curtiss-Wright's DCP-122 Single Board Computer.

Rate Sensor Assembly (RSA)

The RSA Single-axis is a high performance, low-cost successor to troublesome mechanical gyros based on a single-axis Fiber Optic Gyro (FOG). The all-fiber gyro – with no moving parts to wear out or fail – ensures high reliability, superior performance, and exceptional vibration, shock, and acceleration survivability.

SwitchBox – Gigabit Ethernet Switch Module

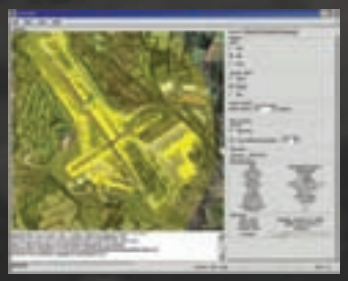
The SwitchBox delivers 20 Gigabit (GigE) ports in a single slot rugged chassis. This ready to deploy rugged GigE multi-layer switch enables fast, reliable, and deterministic forwarding (switching and routing) of control and data packets with up to 20 wire-speed 10/100/1000-Mbps interfaces that can be used to connect multiple chassis, cards, or even processors with in platform networks.

Mission Computer

Curtiss-Wright's Mission Computer system provides high-performance mission compute power for a wide variety of ground, air, sea and aerospace platforms. The Mission Computer is powered by four Curtiss-Wright PowerPC SBCs.

RVP Plot Extractor

Curtiss-Wright's RVP Plot Extractor receives and processes primary radar video to identify candidate targets of interest and distribute the plot data over an Ethernet local area network (LAN). Configured as either single or multi-channel variants, RVP Plot Extractor systems are available in industrial grade rack-mounted units, naval-qualified enclosures, or alternatively as board-level solutions for OEM integrators.



RVP Radar Distribution

The standard RVP Radar Video Distribution configuration is a 4U rack-mount industrial-grade enclosure. This system is based on high-performance Pentium hardware processors running the embedded RVP application software on power-up. A rugged flash disk is used to enhance reliability and tolerance of operating temperatures.

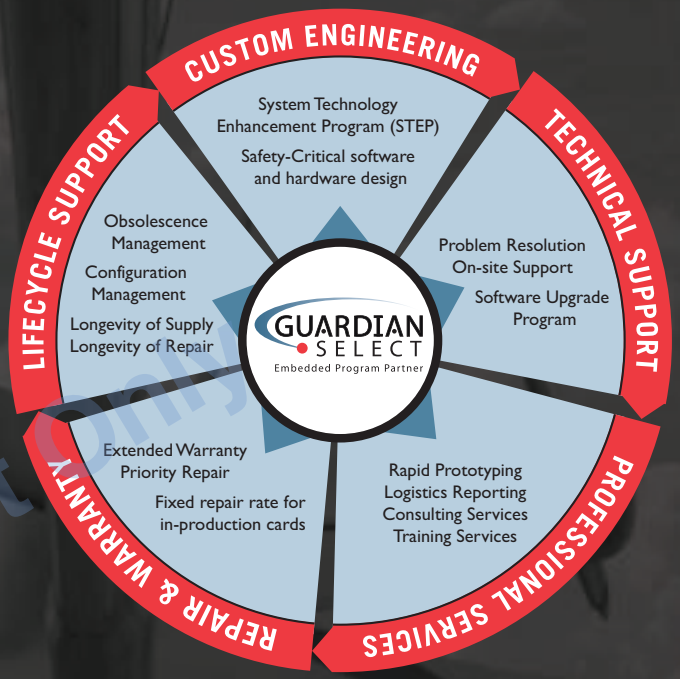
Sentric

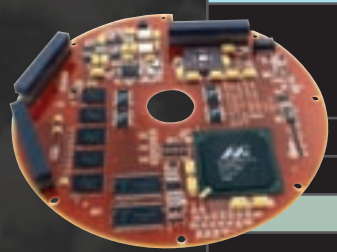
Sentric is a high-resolution, screen recorder that captures, compresses and digitally stores one or more channels of high-resolution RGB computer video, composite TV and audio. Building on success with previous generations of screen recording solutions, Sentric is a fully digital screen recording solution, even capturing digital video (DVI) if required.

Guardian Select™ Services

Curtiss-Wright Controls Embedded Computing has over 20 years experience providing high-performance, open architecture, embedded processing solutions for real-time, high-reliability applications. This experience forms the cornerstone of Curtiss-Wright's comprehensive Guardian Select suite of services.

The intent of Guardian Select is to deliver total service and support to system developers throughout the life of their program. The Guardian Select services program provides service offerings that can be tailored to meet specific customer needs throughout the life of a program. Curtiss-Wright understands that high-quality services are critical to a program's success and we maintain the resources and the expertise to deliver first-class service and support.





Guardian Select Services Offering					
	Last Time Buy Notice	Last Order Date	Last Build Date	Last Repair Date	
NRE					Custom Engineering
IPT & IST Support	Standard Free Support				Technical Support
	Signature Support				
	On-site Support				
	Software Upgrade Program				
	Program Management				Professional Services
Rapid Prototyping					
Quality Reports/Traceability					
Training & Consulting					
	STD WTY (1 year)	Out of Warranty Repair			Repair & Warranty Services
		Extended Warranty			
		Priority Repair			
	Variant Creation				Life-cycle Support
	Configuration Management				
	Obsolescence Reports		Longevity of Supply/Repair		
			Longevity of Repair		
Early Access Units	Production (5-7 yrs)	Last Time Buy (up to 1 year)	End of Life (1 year)	Obsolete	

Guardian Select™ Services

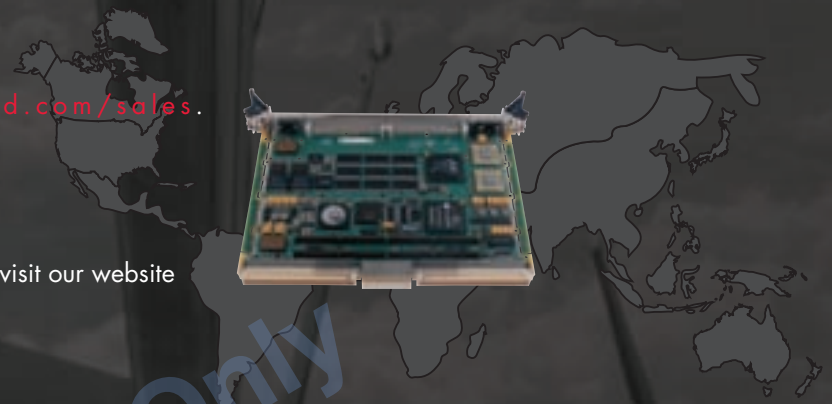
GUARDIAN SELECT
Embedded Program Partner

Service	Description
CUSTOM ENGINEERING	
NRE Development	NRE development.
TECHNICAL SUPPORT	
Signature Support	Signature Support provides customers with priority service and an extended support scope. Technical support for select Curtiss-Wright products is limited (Graphics, FPGA, Linux & Integrity). For these products technical support is provided via Signature Support after the limited support allowance is used.
Software Upgrade Program	Provides upgrades on Curtiss-Wright supplied software via Technet.
PROFESSIONAL SERVICES	
Program Management	Single point of contact to resolve program issues associated with support, manufacturing, engineering, finance, and services.
Rapid Prototype	Provides an easy and effective way to test highly complex software and hardware systems early in the design cycle. Helps designers to simplify user interfaces, visualize product operation, refine functional requirements, and identify potential technical and performance problems before the product is released.
MTBF Report	Outlines the average time between equipment failures over a given period.
FMECA Report	A Failure Modes, Effects and Criticality Analysis (FMECA) report identifies the most likely types of failures and their effect upon the product. FMECA is used with the MTBF reliability analysis to assist in overall system design and to make predictions of future logistics requirements.
REPAIR & WARRANTY	
Extended Warranty	Extends Curtiss-Wright's one year hardware warranty an additional year. Must be purchased at the time of order placement.
Priority Repair	Next on bench repair service expedites repair turn around. Can be ordered via the Return Material Authorization (RMA) form at the time of board return.
LIFECYCLE SUPPORT	
Level 1 Configuration Management	Major and Minor changes are provided for information purposes. Change approval authority rests with Curtiss-Wright. Offered on standard product as well as customer-specific variants. Engineering Change Orders are provided on a quarterly basis.
Level 2 Configuration Management	Adoption of Major changes requires customer approval. Minor changes are provided for concurrence of classification. Available for customer-specific variants only.
Level 3 Configuration Management	Adoption of both Major and Minor changes require customer approval. Available for customer-specific variants only.
Customer Specific Variant	Customer-specific variant creation. Prerequisite for Level 2 and Level 3 Configuration Management Services.
Obsolescence Reports	An on-going and forward-looking status of the Integrated Circuit (IC) components on the customer's Curtiss-Wright product.
Longevity of Supply	Sustain tools, test equipment, and expertise for continued builds and repairs. Requires component purchases that are separate from this service to sustain build and repair quantities.
Longevity of Repair	Sustain tools, test equipment, and expertise for continued repairs. Requires component purchases that are separate from this service to sustain repair quantities.

Guardian Select is the umbrella for all value-added services that Curtiss-Wright Controls Embedded Computing offers to its customers.

Contact a Sales Representative

For a product-specific sales contact in your area, please visit www.cwcembedded.com/sales.



Learn More About our Products

For more information on our broad range of high-integrity computing solutions, please visit our website at www.cwcembedded.com.

Experience the Embedded Battlefield

At www.embeddedbattlefield.com you can view the subsystems and board-level solutions that makeup the operational units on the field. It's an immersive and entertaining experience.

Get Up-to-Date with The Embedded Reporter

The Embedded Reporter will keep you up-to-date on all the latest news about Curtiss-Wright Controls Embedded Computing and alert you to what's coming up in the future, whether it's new product announcements or major program wins. If you'd like to receive quarterly updates from us via e-mail, then you'll want to subscribe to our Embedded Reporter e-newsletter at www.cwcembedded.com/reporter. If, however, you prefer up-to-date information the minute it's available then consider adding our Embedded Reporter RSS feed to your news reader. Learn more about RSS and grab our feed at www.cwcembedded.com/rss.

Gain Business Insight with CW-TV Videos

Curtiss-Wright Controls Embedded Computing's CW-TV offers valuable information emerging from the embedded marketplace. Watch a video now at www.cwcembedded.com/cwtv.

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